Integrated Circuits: The Problem with Wires (and Some Solutions)

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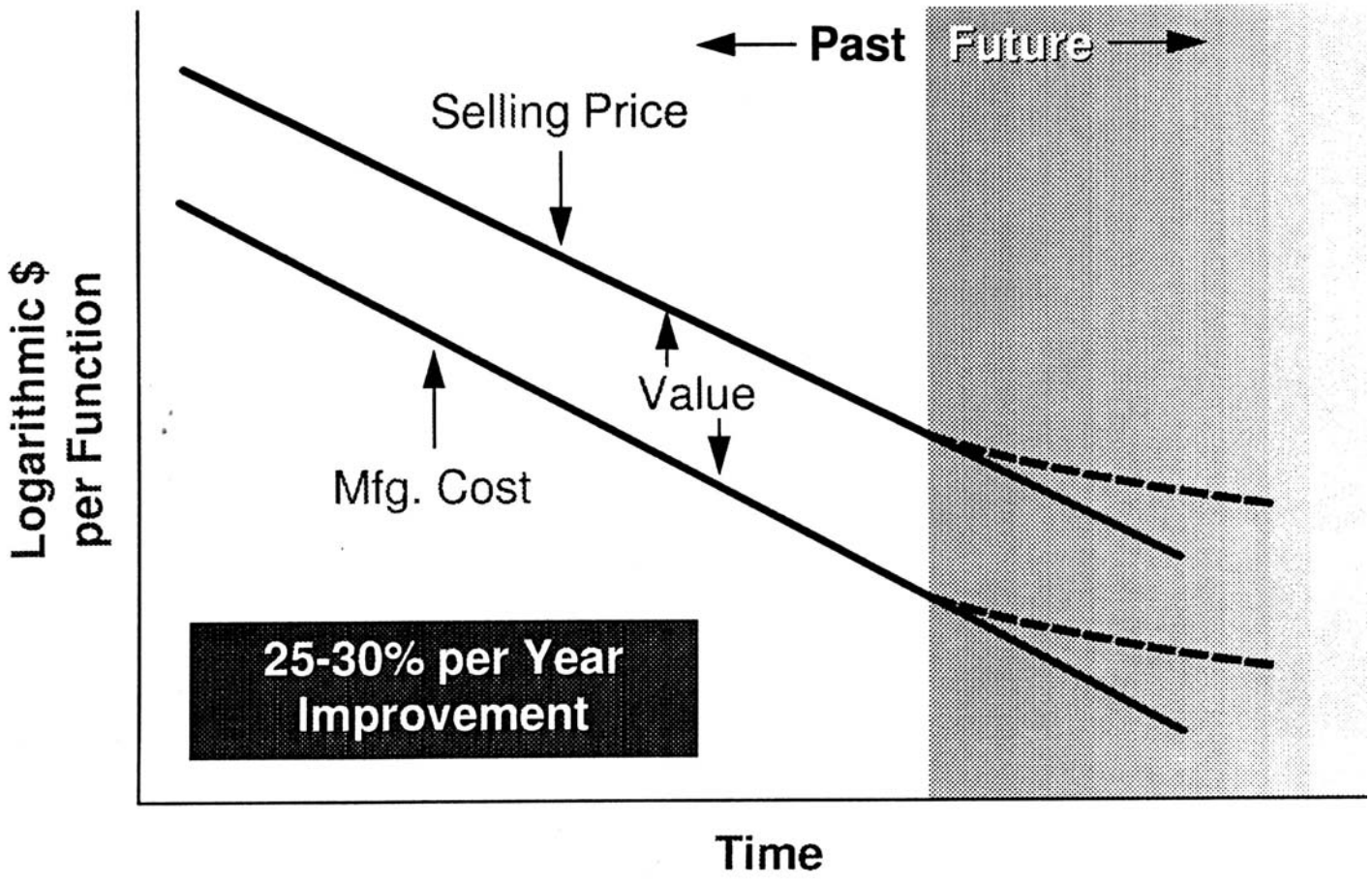
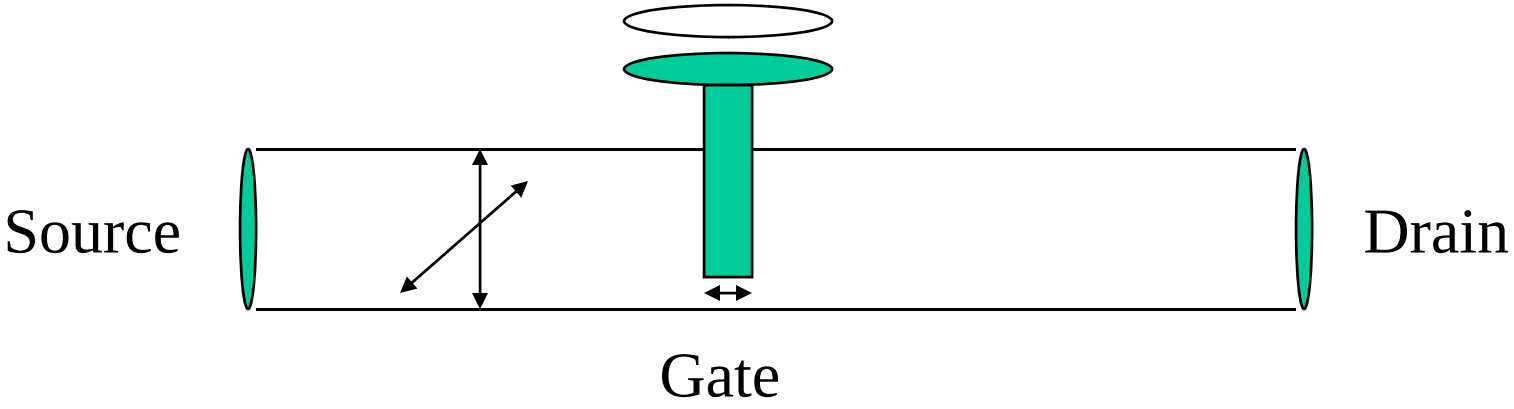
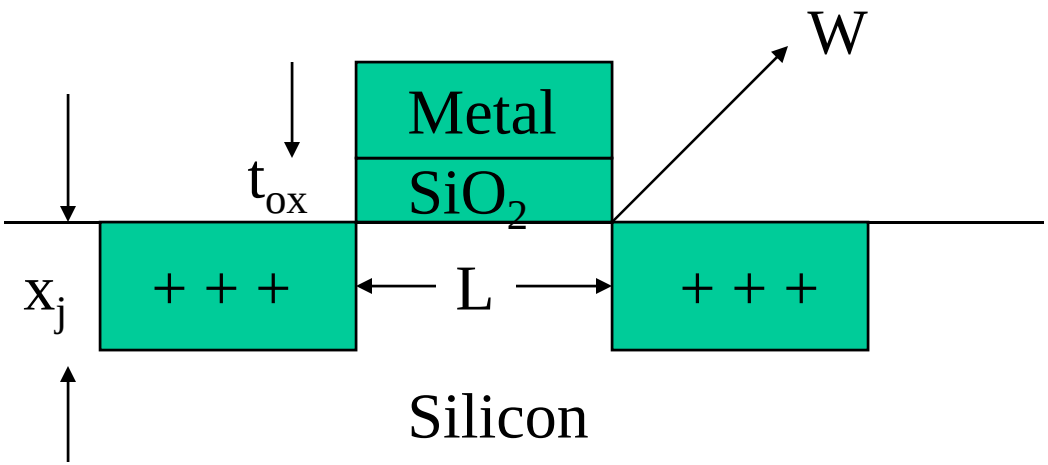
Strategy Based on Maintaining Historic Cost Improvements



Four Parameters (L, W, x_j, t_{ox})





Scaling Parameters for CMOS

* **Parameter**	* **S Factor S~1.15**
* W, L, T_{ox}, X_j	* 1/S 87%

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* Delay	* 1/S	87%

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* Die Size	* S_c	115%

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* Power	* $1/S^2$	76%
* Energy	* $1/S^3$	66%
* Die Size	* S_c	115%
* Number per Die	* $S^2S_c^2$	175%

$$C_{ox} = \varepsilon \frac{WL}{T_{ox}} = \frac{1/S \; 1/S}{1/S}$$

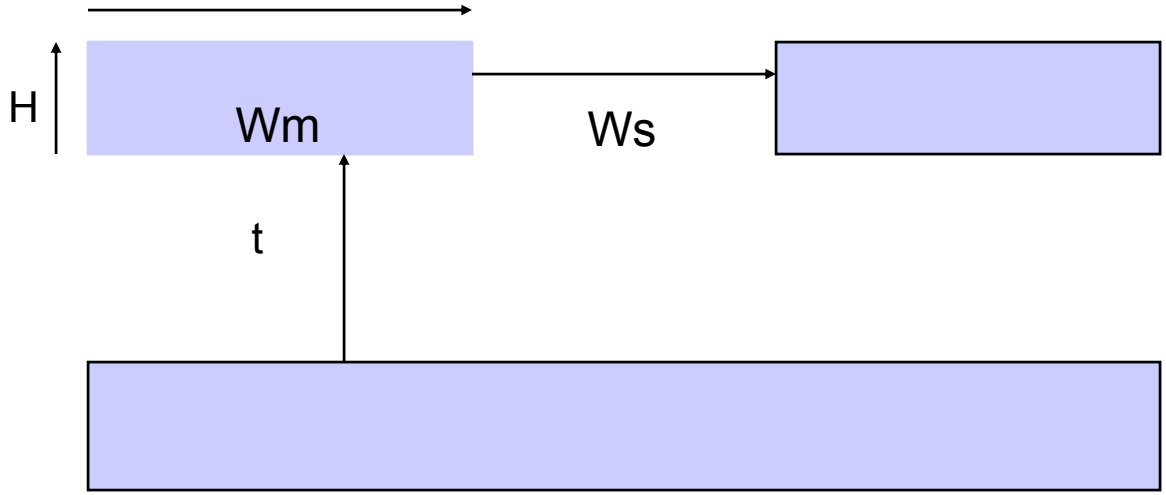
$$I = \mu \frac{C_{ox}}{A} \frac{W}{L} \frac{V^2}{2}$$

$$\tau = C_{ox} V / I$$

$$P = IV$$

$$E = P\tau$$

Interconnection Scaling



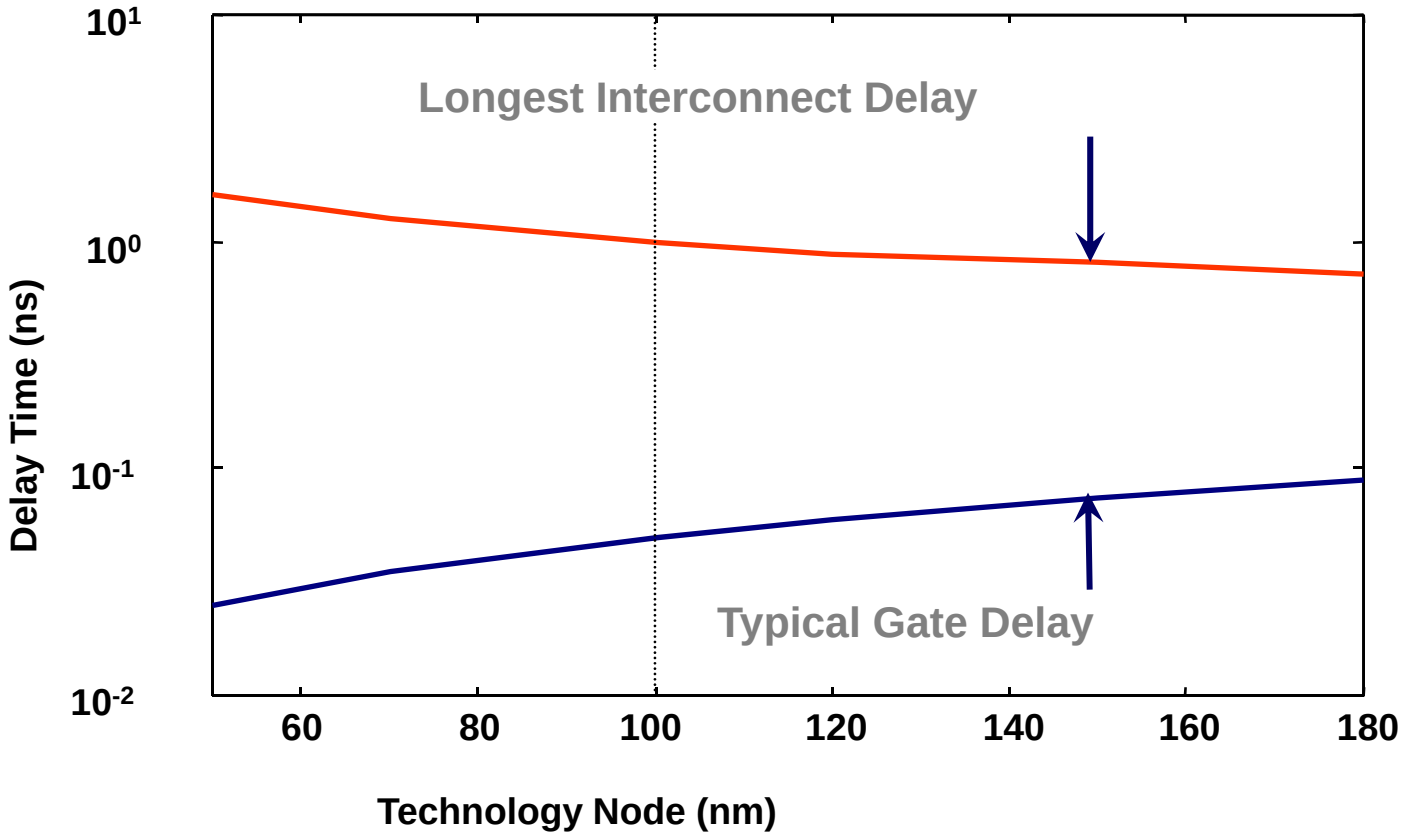
Scaling Parameters for Interconnections

* **Parameter**	**S Factor**	**S~1.15**
* Wm, Ws, H, L, t	* $1/S$	87%
* Resistance/L = $\rho/W_m H$	* S^2	132%
* Local Length, L	* $1/S$	87%
* Local RC Delay = RCLL	* 1	100%
* Die Size	* S_c	115%
* Global RC Delay = RCS_c^2	* $S^2S_c^2$	175%

Problems with Scaling

1. Global Wiring Crisis

The Problem with Wires



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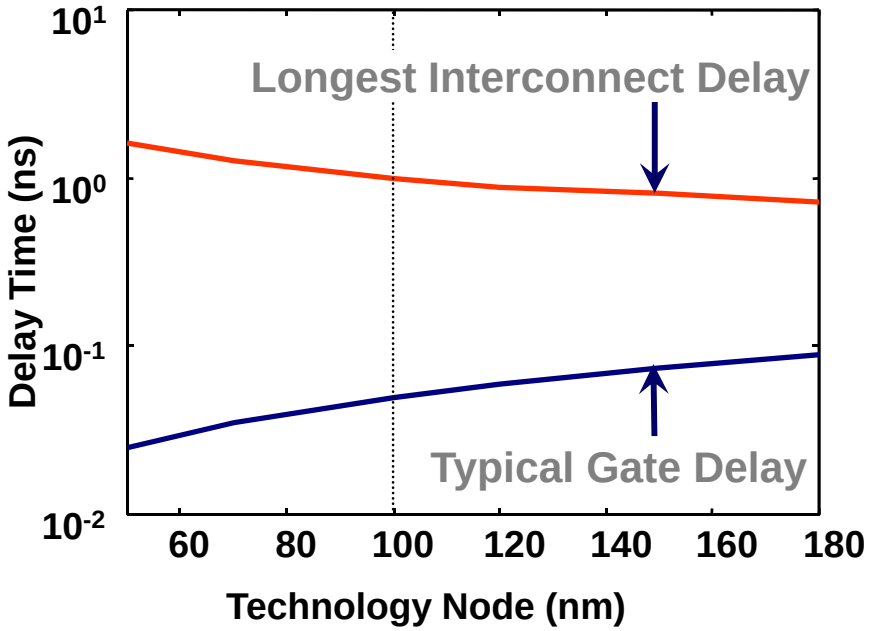

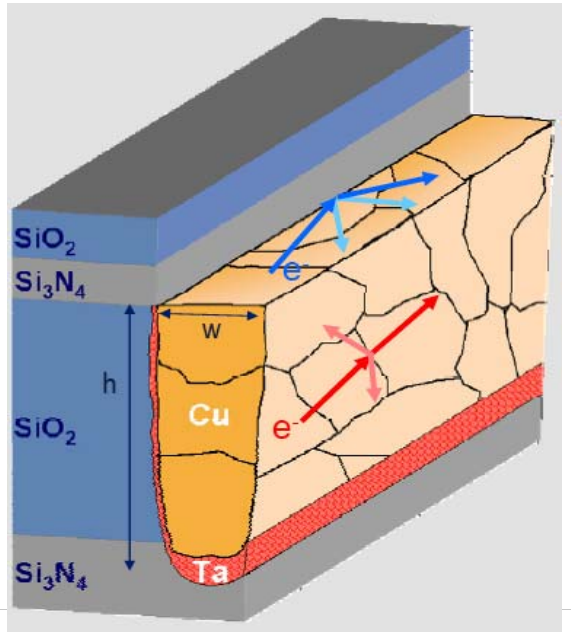

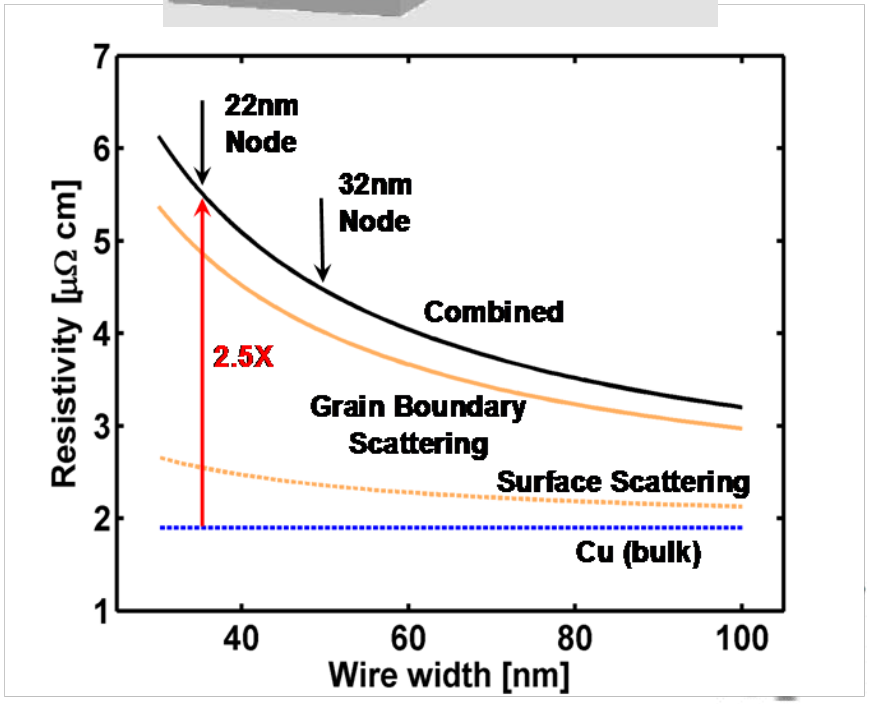

Scaling Parameters for Interconnections

* **Parameter**	**S Factor**	**S~1.15**
* Wm, Ws, H, L, t	* 1/S	87%
* **Resistance/L > ρ/W_mH**	* **$5S^2$**	**x132%**
* Local Length, L	* 1/S	87%
* **Local RC Delay = RCLL**	* **5**	**500%**
* Die Size	* S_c	115%
* Global RC Delay = RCS_c^2	* $S^2S_c^2$	175%

Problems with Scaling

1. Global Wiring Crisis
2. Local Wiring Crisis

ITRS projections and Industry Roadmap

2007 ITRS	2010 45 nm	2013 32 nm	2016 22 nm	2019 16 nm
Off-chip BW (GHz)	15.1	23.0	39.7	62.4
Package Pin Count (Cost-Effective)	2783	3704	4930	6562
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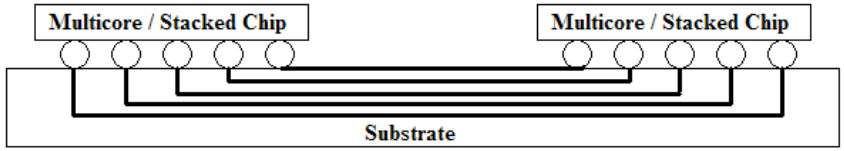
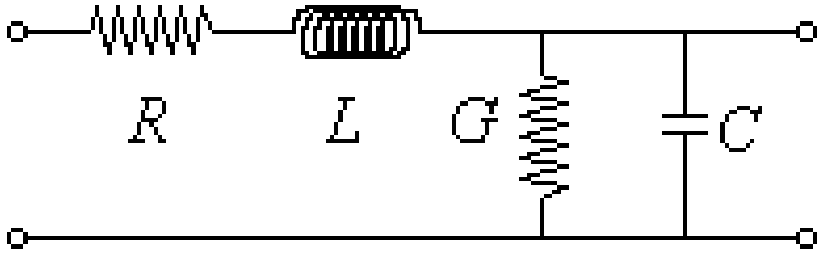
Max Chip Power	198	198	198	198





- Exponential decay and change in magnitude and phase of signal
- Resistance (R) and Inductance (L) governed by metal properties
- Capacitance (C) and Shunt Conductance (G) governed by insulator properties

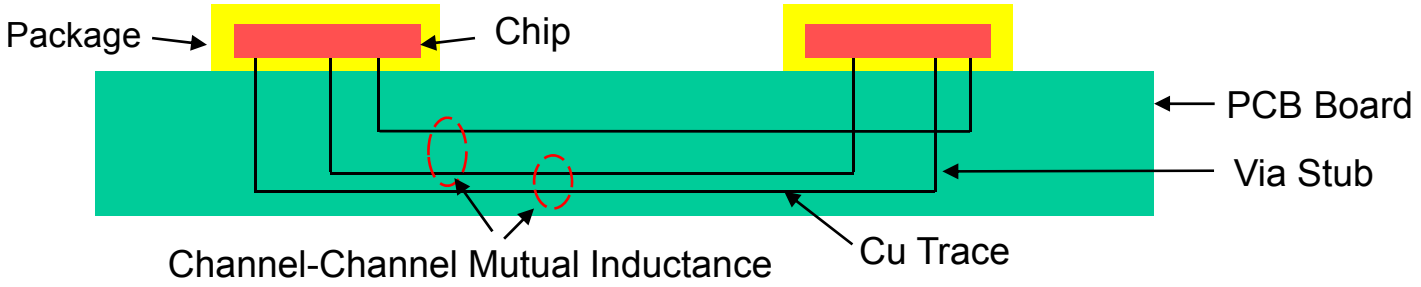
$$E = E^{-} e^{-\gamma z}$$

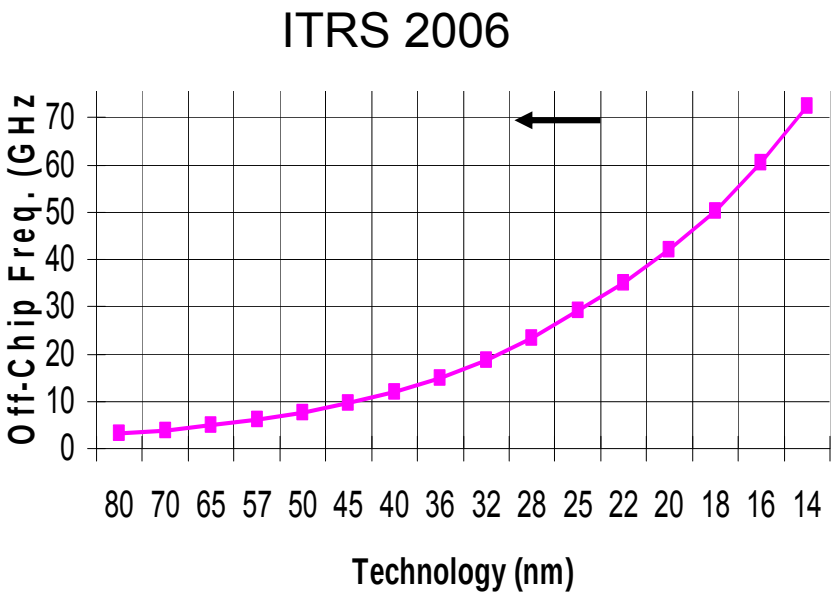
$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$$

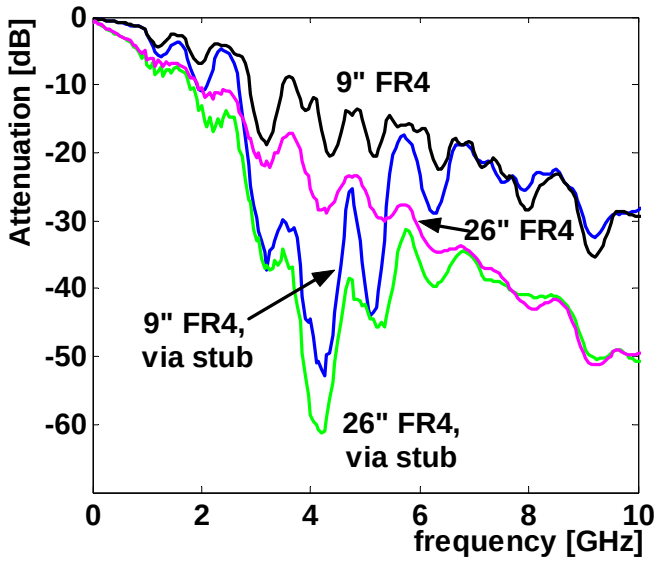
$$\alpha_c = \frac{\sqrt{\frac{\omega \mu_0 \varepsilon_r}{2\sigma \mu_r}}}{\eta_0 d}$$

$$\alpha_d = \frac{\omega \sqrt{\mu_r \varepsilon_r} \tan \delta}{2c}$$

Off-Chip Bandwidth







Problems with Scaling

1. Global Wiring Crisis
2. Local Wiring Crisis
3. Off-chip Wiring Crisis

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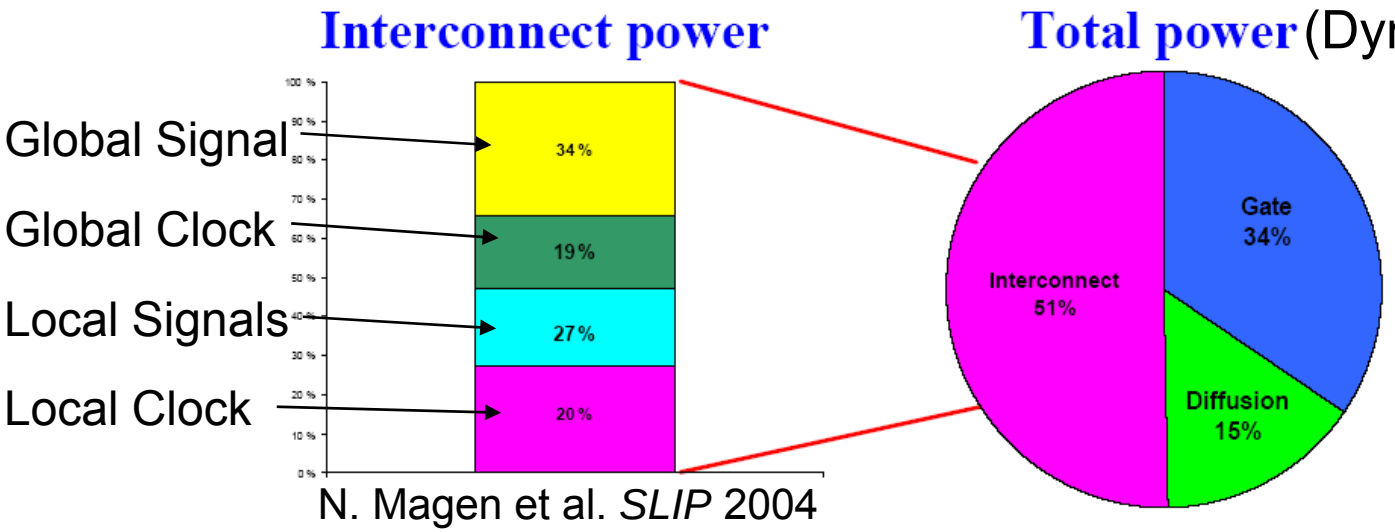


N. Magen et al. *SLIP* 2004

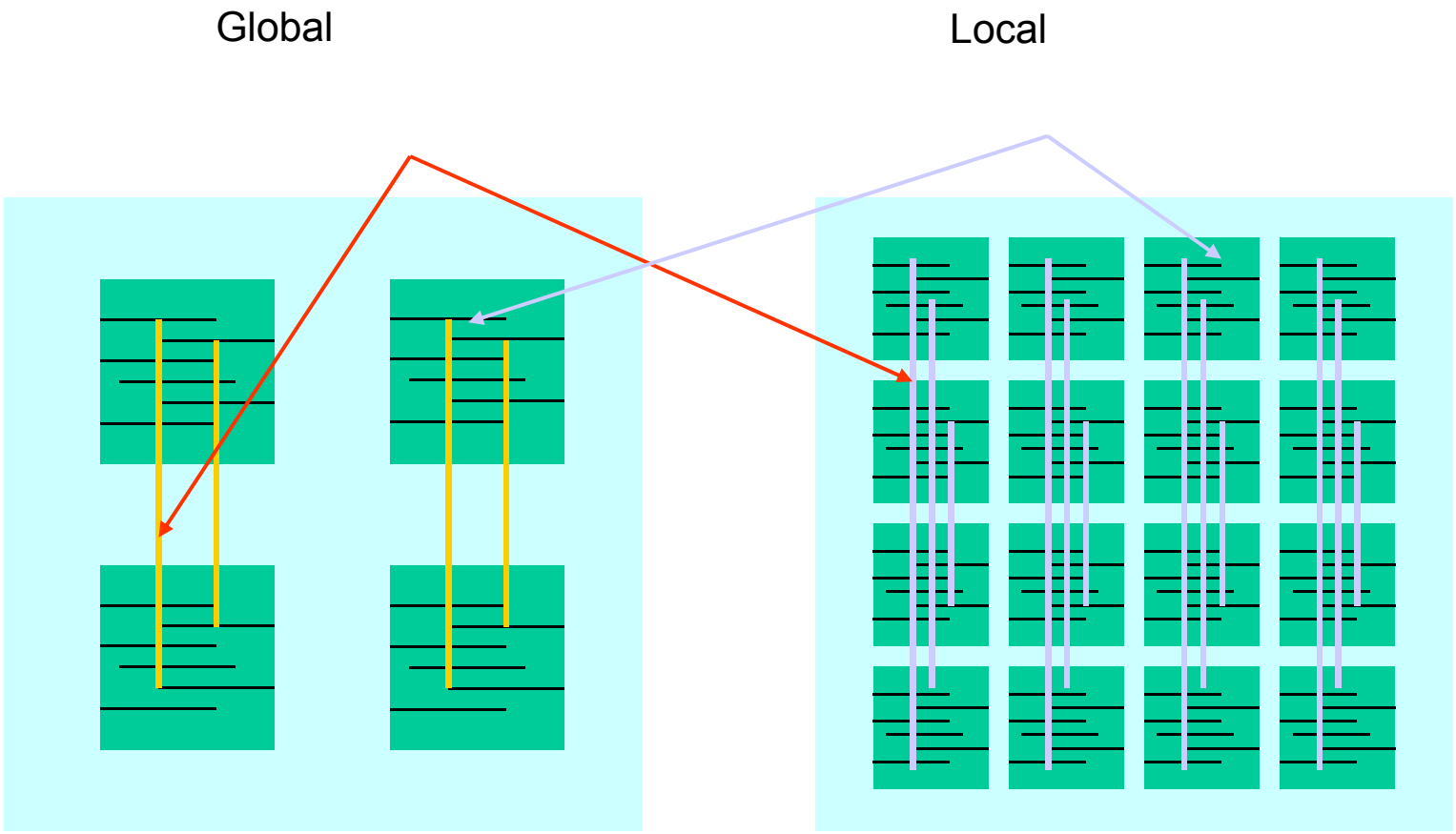
130 nm µP

- Interconnects: >50% dynamic pwr

Problems with Scaling

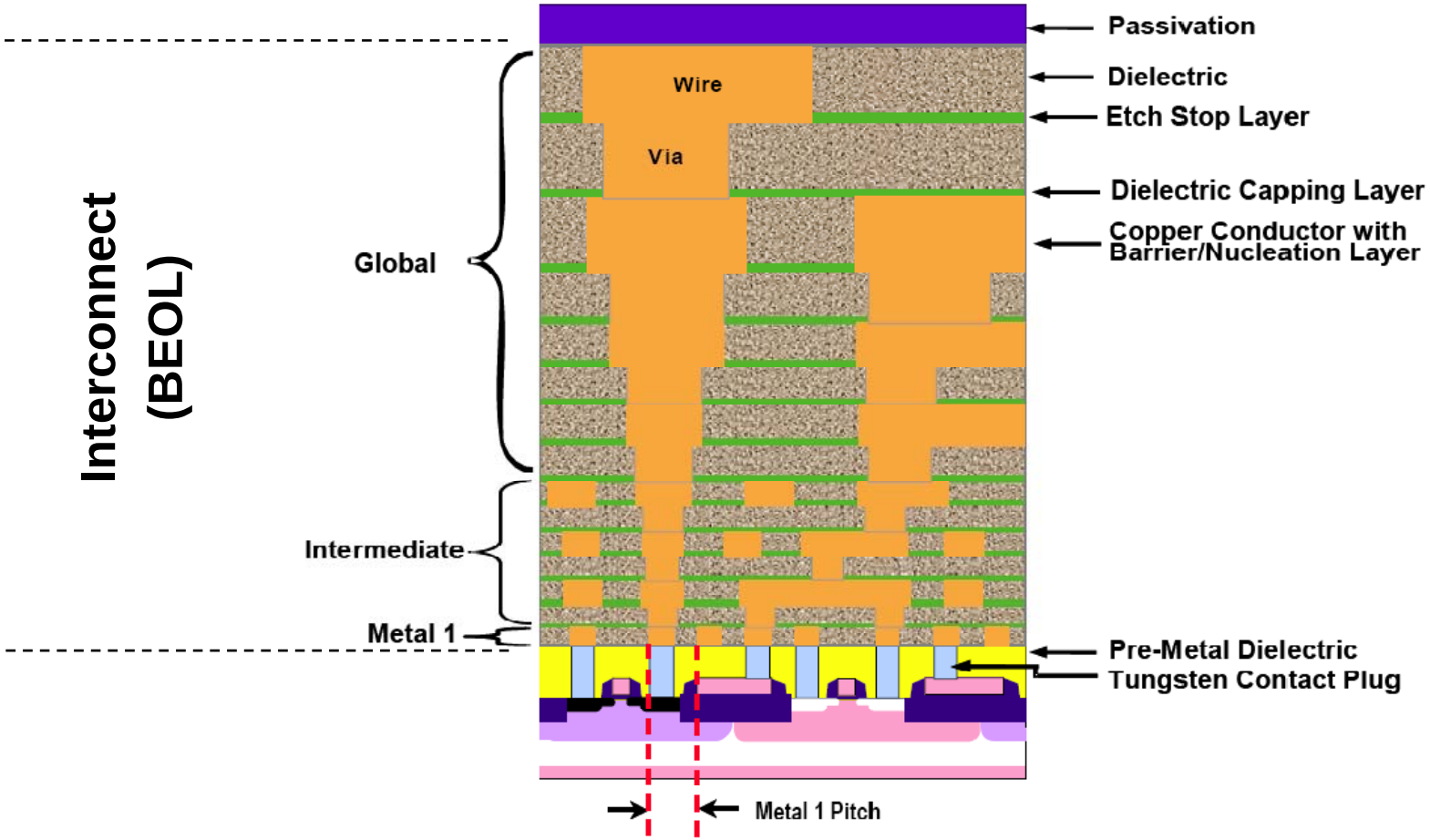
1. Global Wiring Crisis
2. Local Wiring Crisis
3. Off-chip Wiring Crisis
4. Power limitations: V_{dd} and t_{ox} are not scaling
   - » Power is now *everything*
   - » Heat: Steady-state operation no longer possible

Shorter Wires and Cooler Transistors

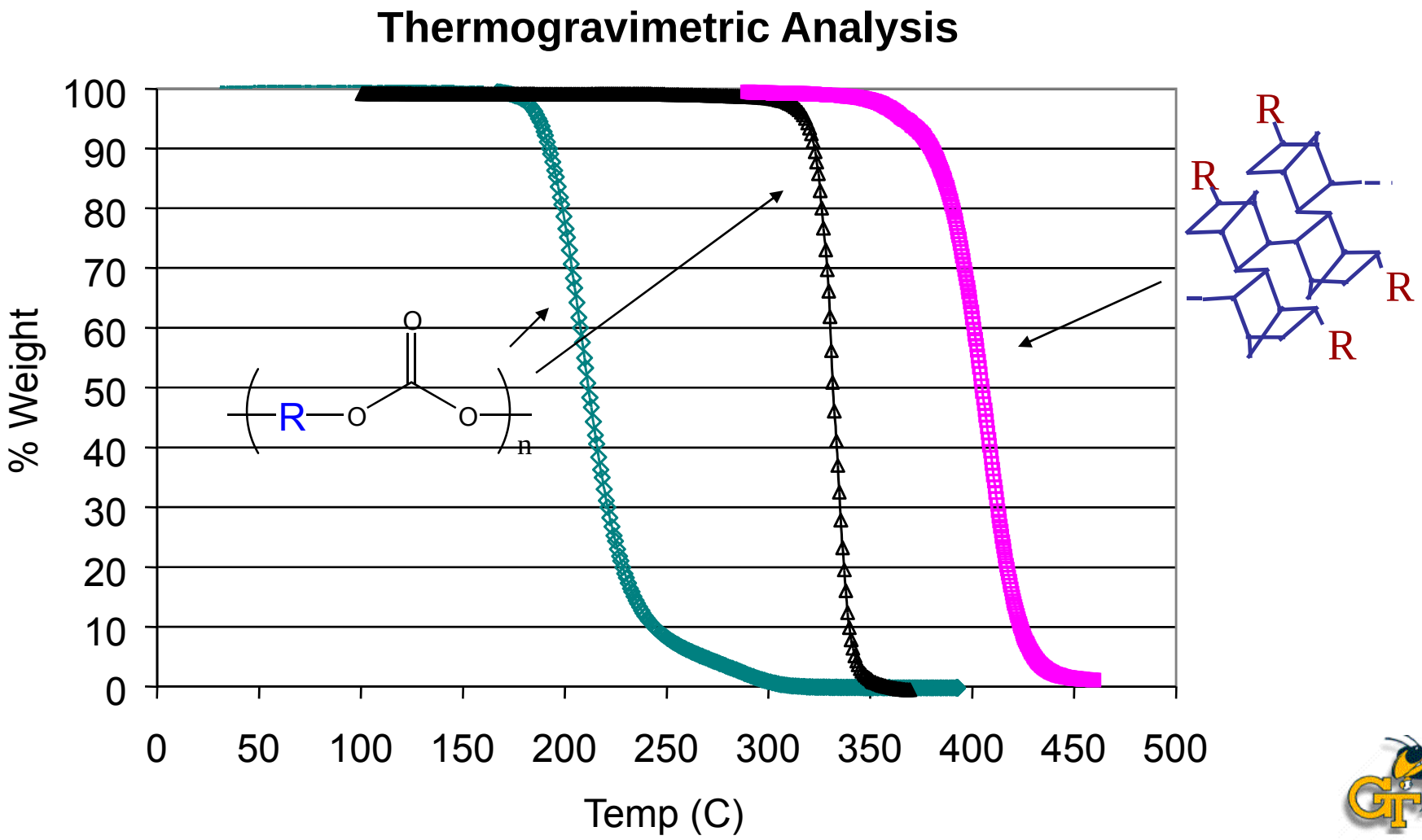


On-Chip Ultra Low-k

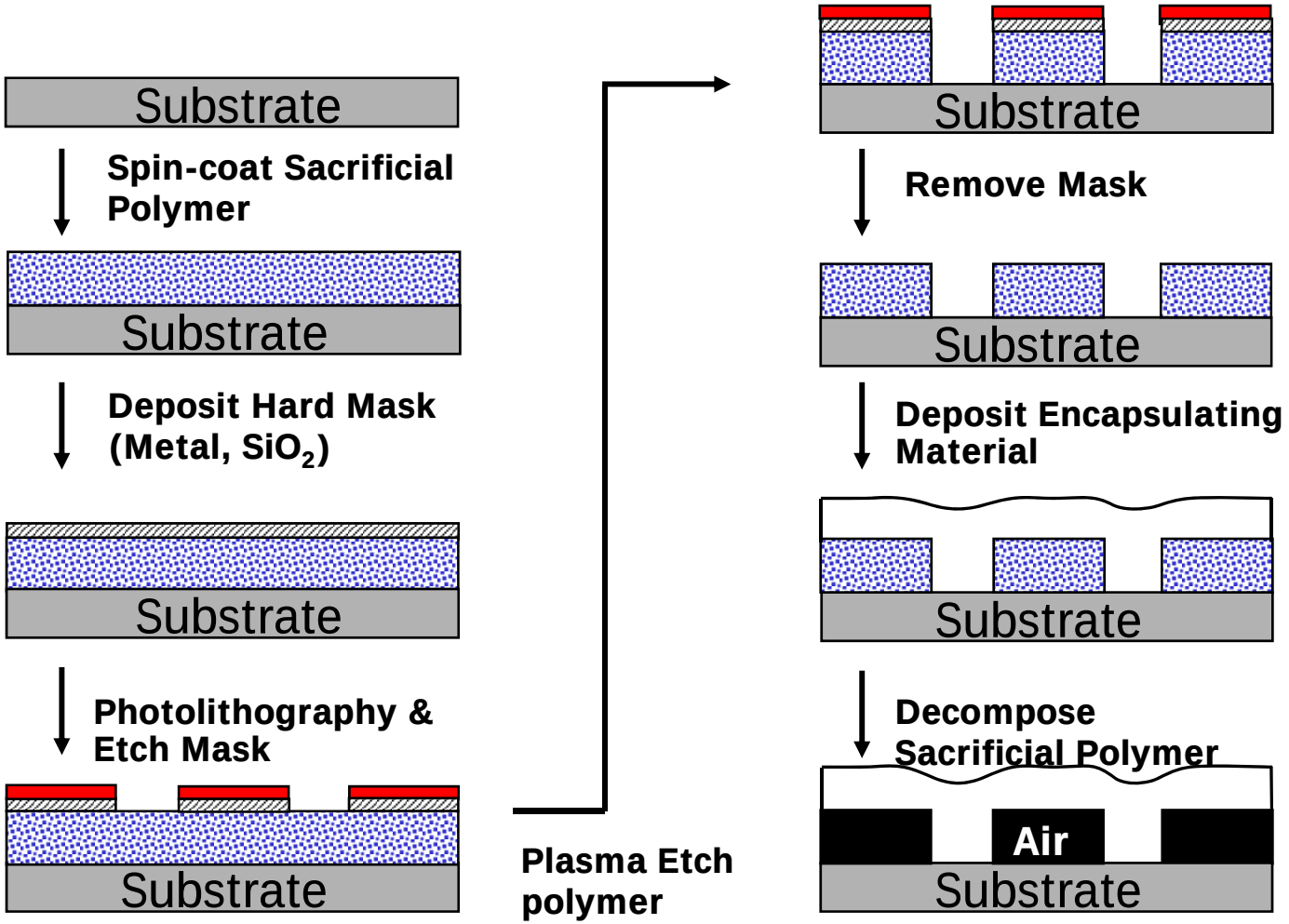
Cross-section Interconnect Structure



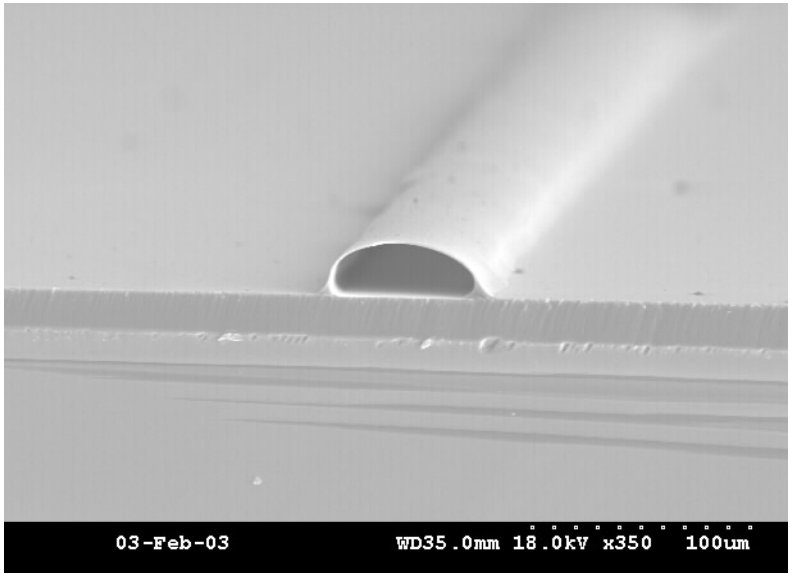
Sacrificial Materials

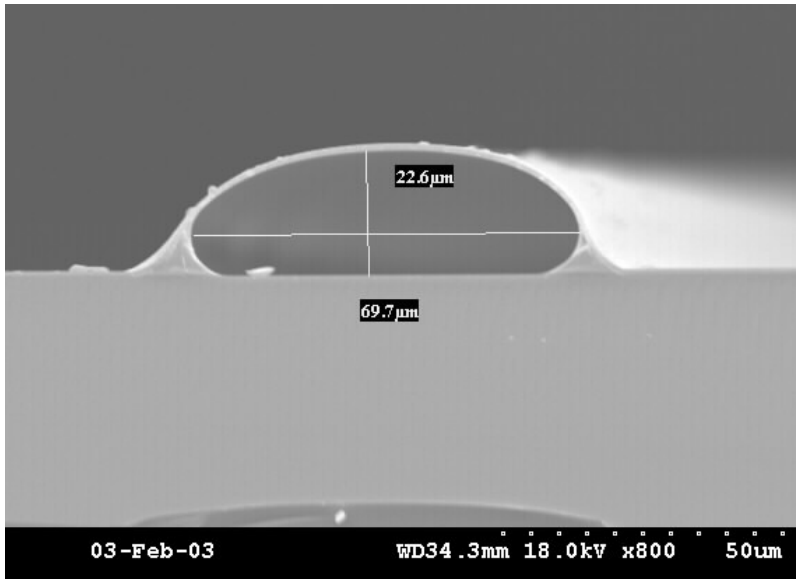


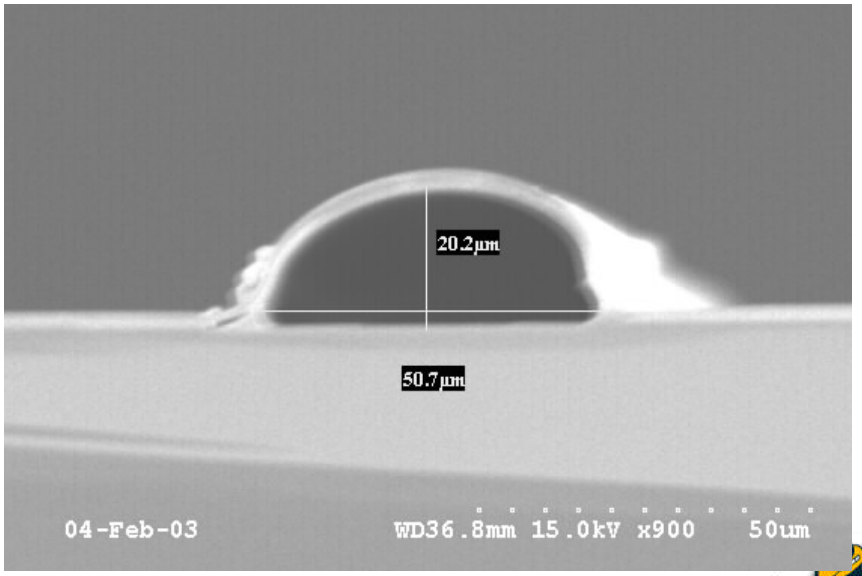
Non-Photosensitive Fabrication



Air-Channels in SiO_2



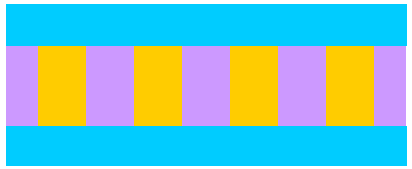




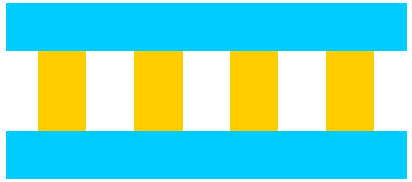
Effective Dielectric Constant (k_{eff})

Standing alone Cu lines **k_{eff}=1.81**

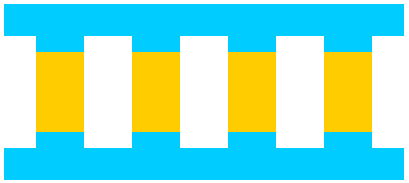
After RIE of SiO_2 **k_{eff}=1.23**



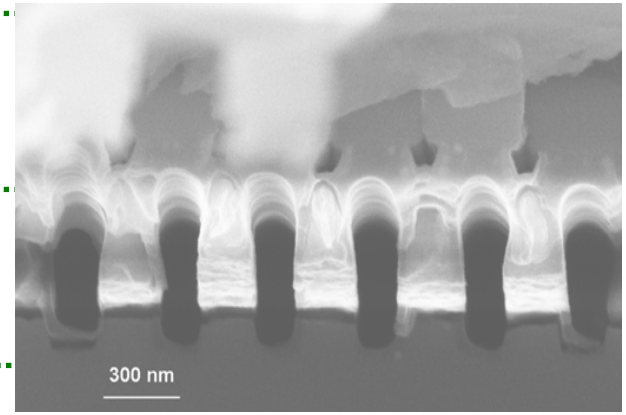
Homogeneous SiO_2 **k_{eff}=4.14**



Air-gaps **k_{eff}=2.42**



Extended air-gaps **k_{eff}=2.17**



- **Width of Cu : 200 nm**
- **Aspect ratio : 1.8:1 (H:W)**
- **Half pitch : 200 nm**
- **Extended height : 80nm(top)/ 100nm(bottom)**
- **Inter-layer dielectric : PECVD SiO_2**

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Todd Spencer

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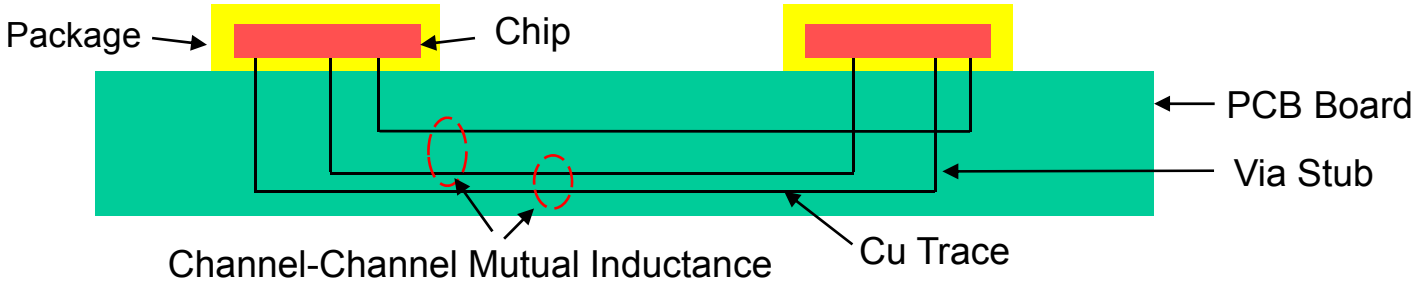
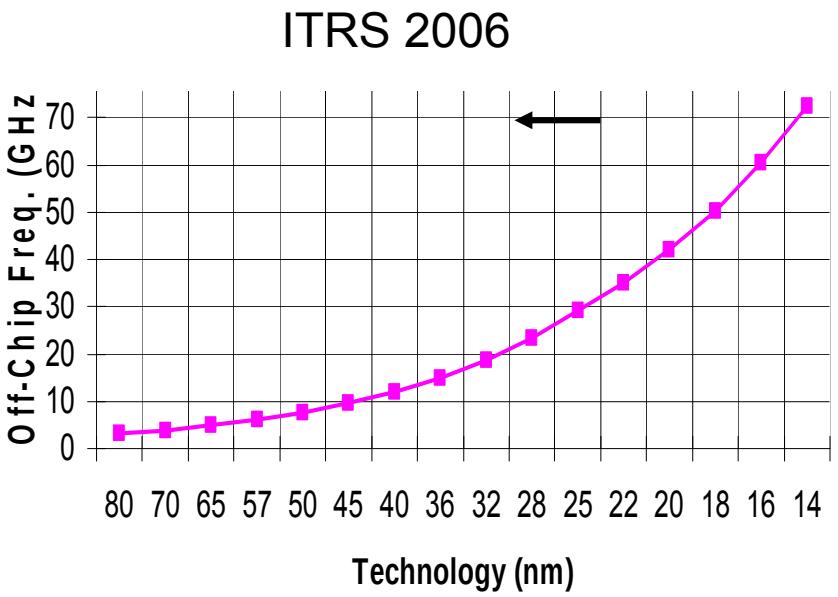
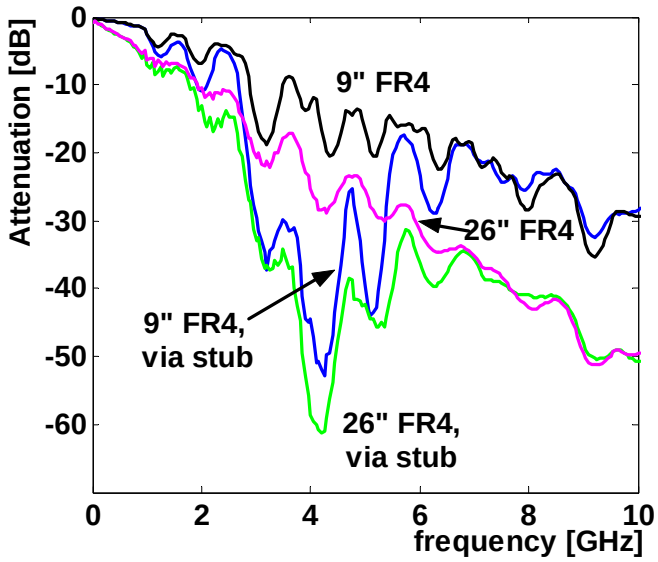






Motivation for Air Insulation on FR4

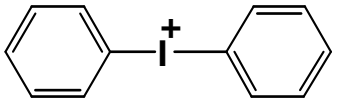
$E/E_o = e^{-\alpha * length}$

* Primary loss due to dielectric in conventional fiberglass-epoxy substrates above 10 GHz
* Conductor loss increases by $freq^{1/2}$
* Dielectric loss scales linearly by *freq*
* Air isolation has lowest ε_r and tan δ
* Signal propagation velocity also increases, lowering latency

$$\alpha_{conductor} = \frac{\sqrt{\frac{\omega \mu_0 \varepsilon_r}{2\sigma\mu_r}}}{\eta_0 d}$$

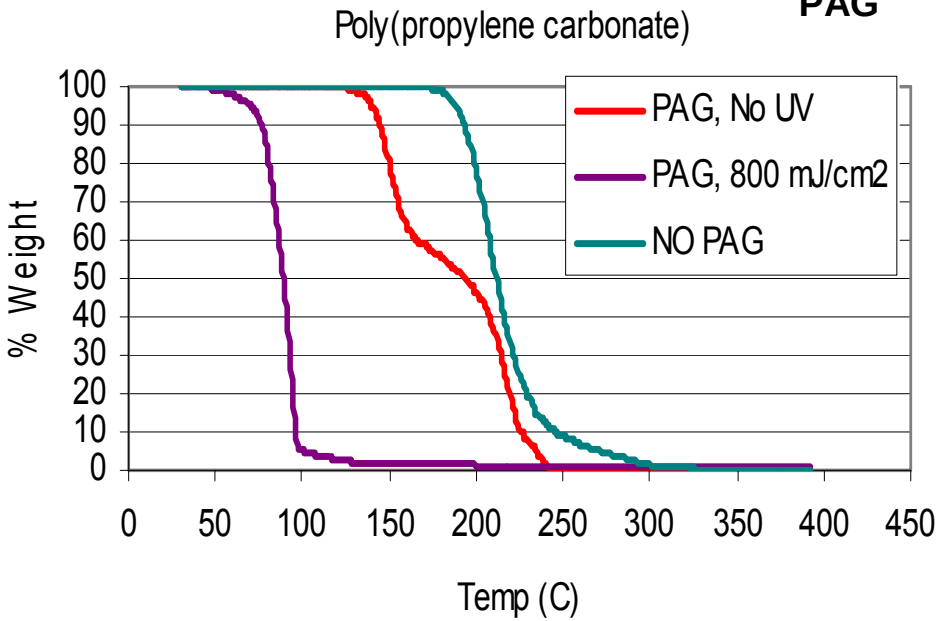
$$\alpha_{dielectric} = \frac{\omega\sqrt{\mu_r \varepsilon_r}\tan\delta}{2c}$$

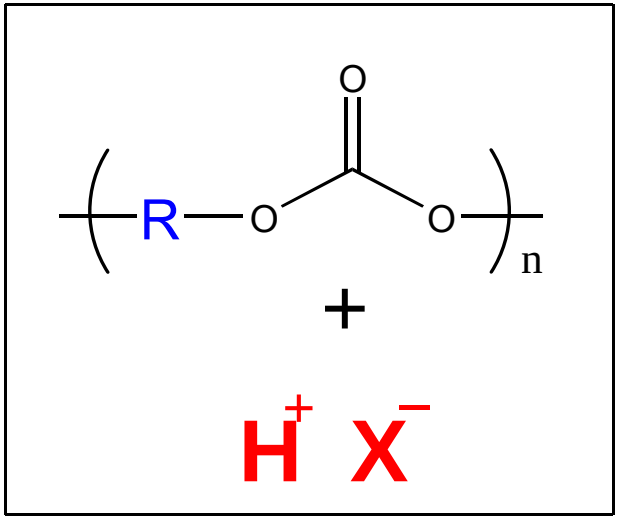
Acid Catalyzed Decomposition



PAG

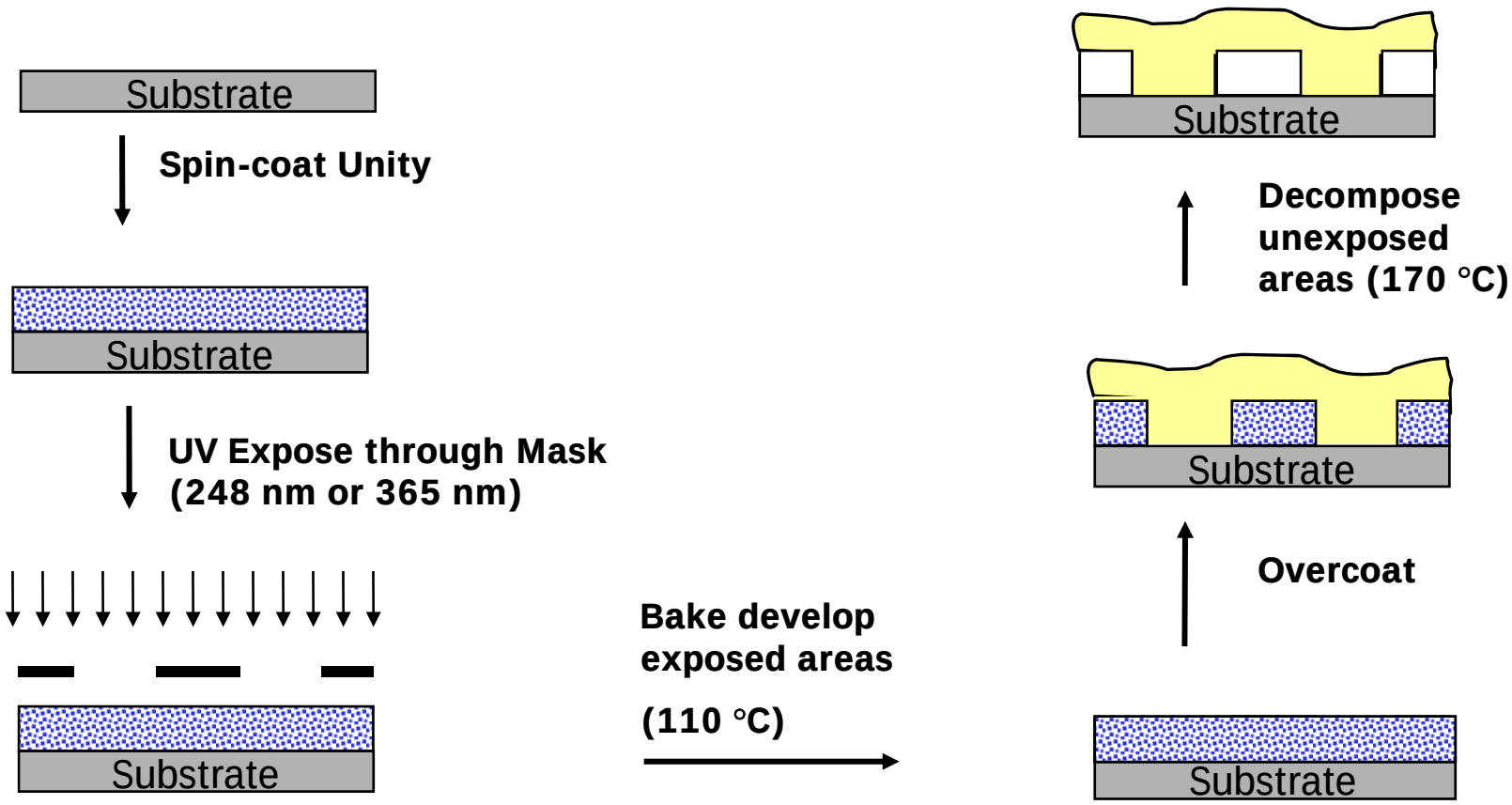
X^- hv or △ → $H^+ X^-$ + Other products



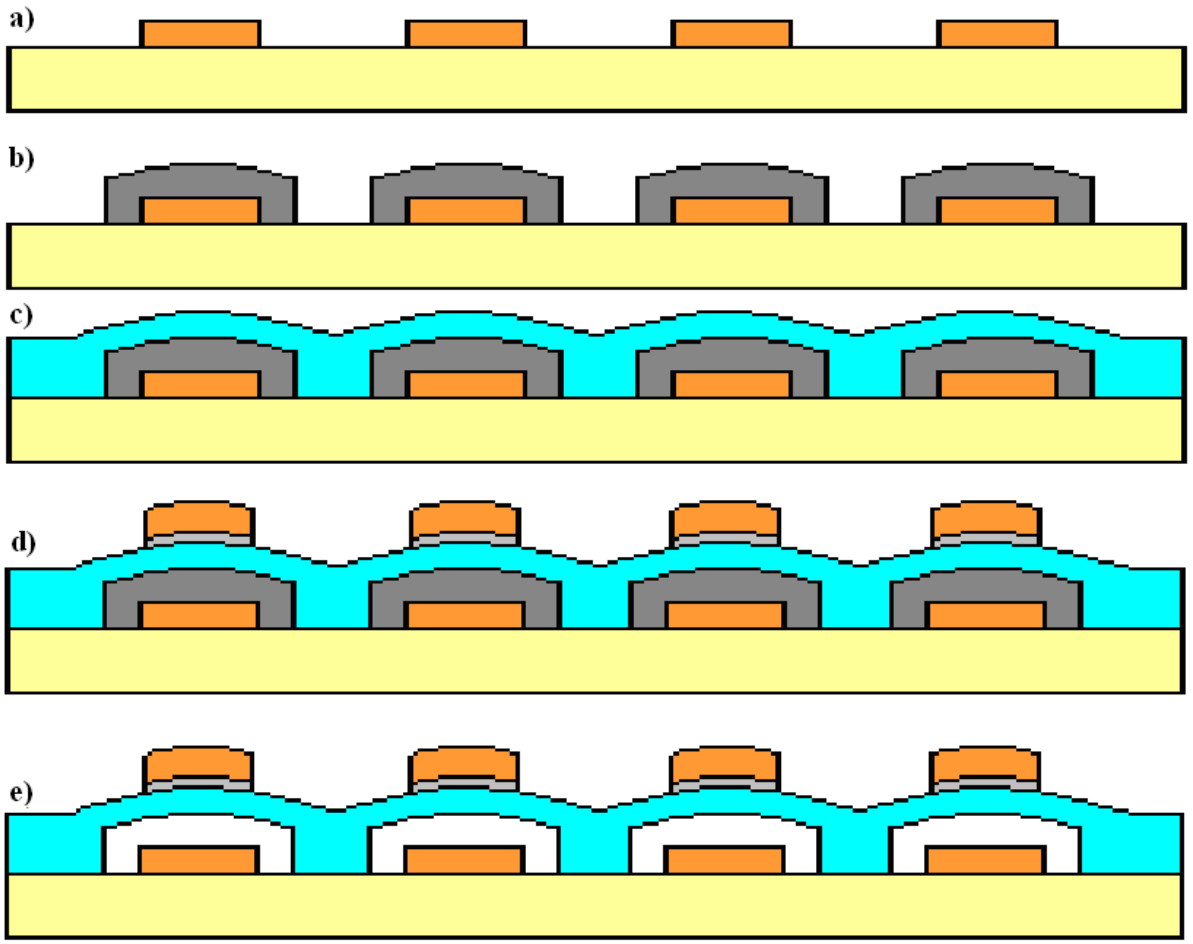


- Acid generation via PAG, aid decomposition onset temperature ~100°C.
- Photo-acid & Thermal acid Generation.

Fabrication of Positive-Tone Sacrificial Polymer

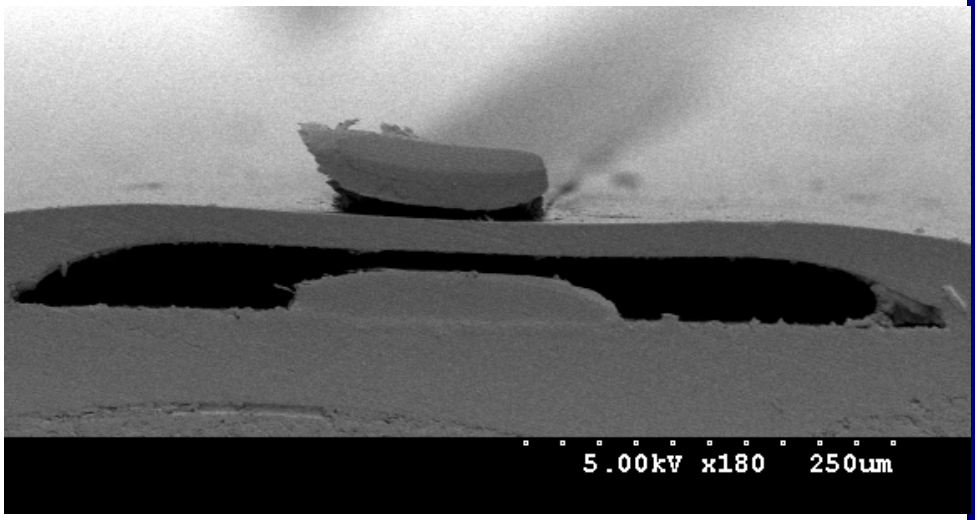


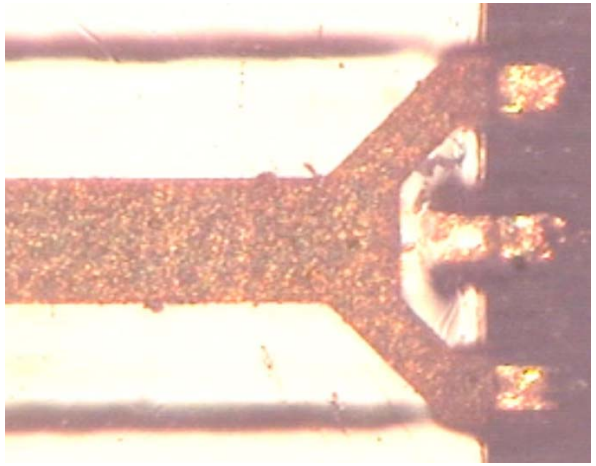
Air-Clad Transmission Lines on Organic Substrates

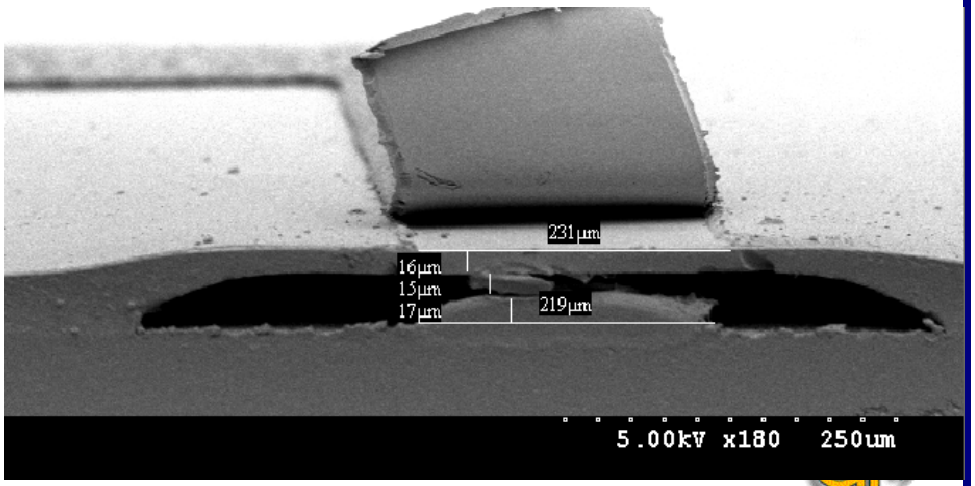


Air-Clad Transmission Lines on Organic Substrates

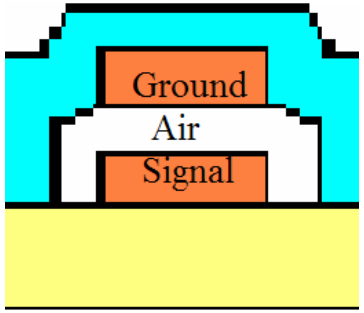
* Parallel plate and suspended ground microstrip lines
* Capacitance reduced by more than 30%
* Loss tangent reduced by more than 85%
* Reduces both conductor and dielectric loss contributions

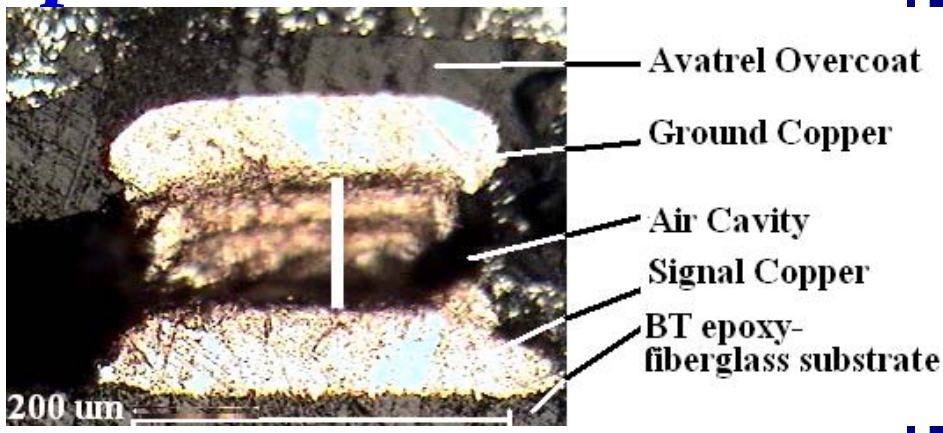






Air Cavity Parallel Plate & Microstriplines



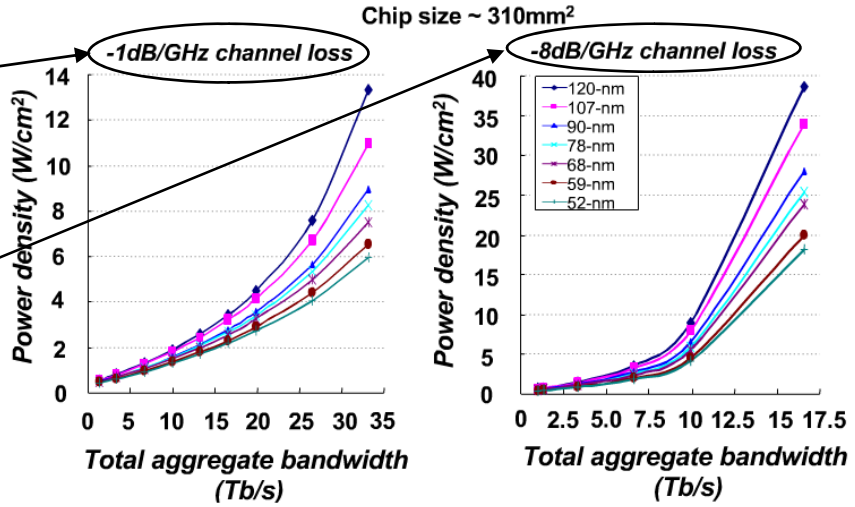


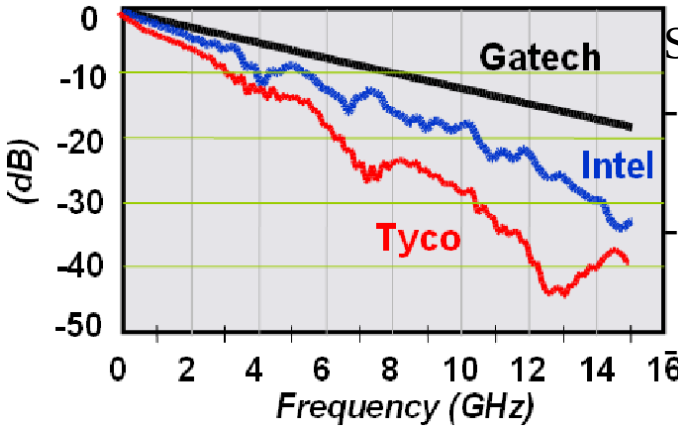
* Air cavity formed between signal and ground lines on FR4
* No polymer between signal and ground (all air)
* Improves on previously reported partial air-gap lines
* Air cavity reduces capacitance by up to 47% for ground line 3x signal line width
* Loss tangent reduced by up to 90%

Ground Line Width (μm)	Capacitance Before Air Cavity (pF)	Capacitance with Air Cavity (pF)	Capacitance % reduction with air cavity
650	16.42	9.02	46.6
650	15.94	10.16	38.0
650	15.29	8.37	46.6
220	12.56	10.27	21.7
220	12.83	10.45	21.5
220	12.85	10.12	25.6

Aggregate bandwidth and energy per bit: channel loss effects

* 1 dB/GHz channel loss allows high aggregate bandwidth at low power density
* 8 dB/GHz loss decreases bandwidth and increases power density
* Channel loss should be as small as possible to minimize energy per bit
* Channel loss can be minimized with air cavity strip



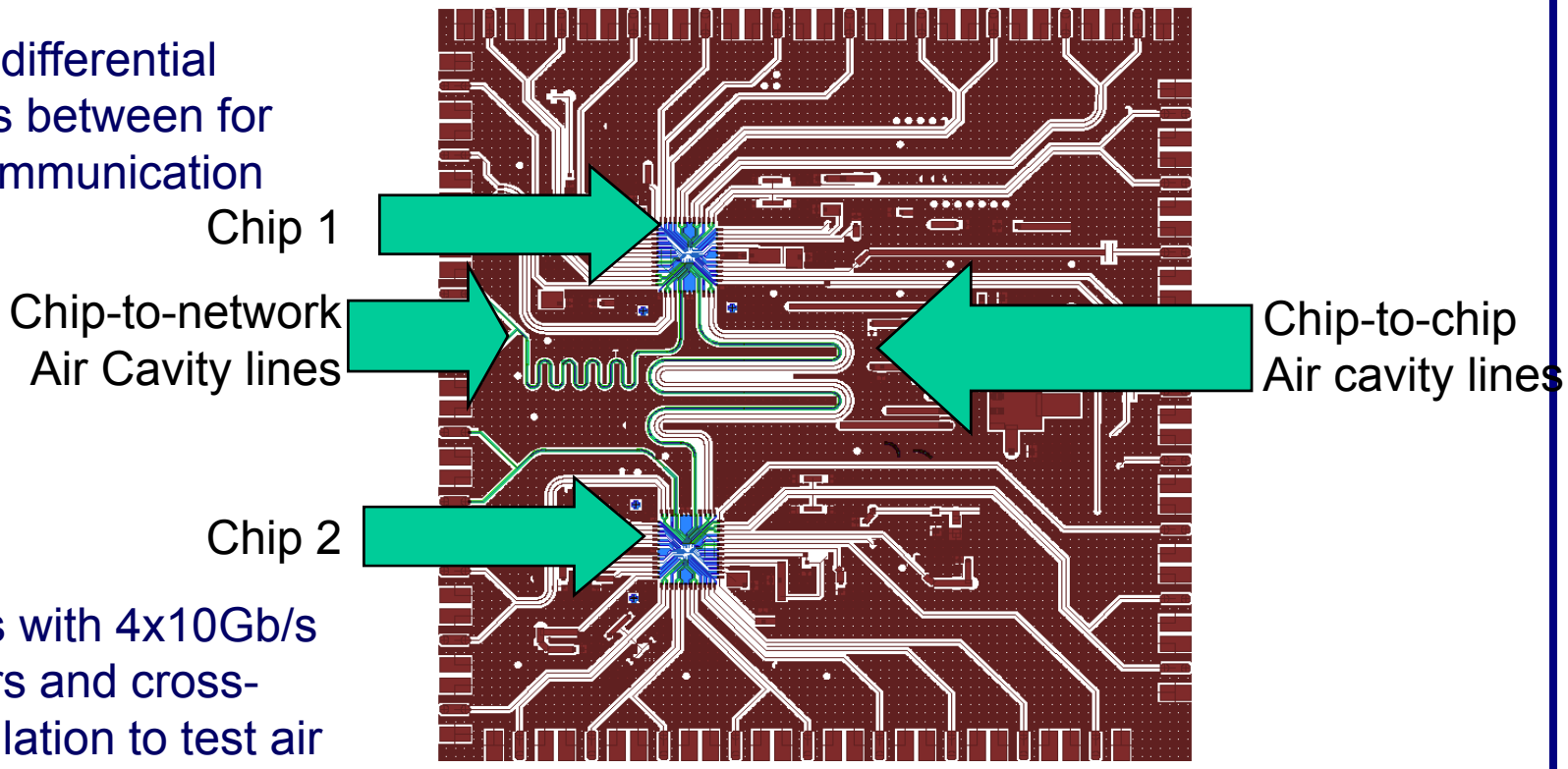


Slope:
-1.2 dB/GHz
-2.1 dB/GHz
-3.3 dB/GHz

Figures courtesy Rizwan Bashirullah, U. of Florida

Air Cavity Lines for Off-chip Communication

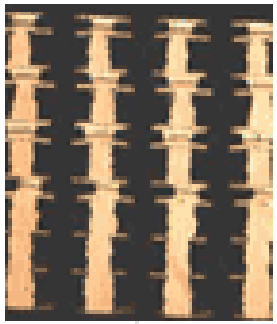
- Research test vehicle designed at University of Florida
- Air cavity differential signal lines between for off-chip communication



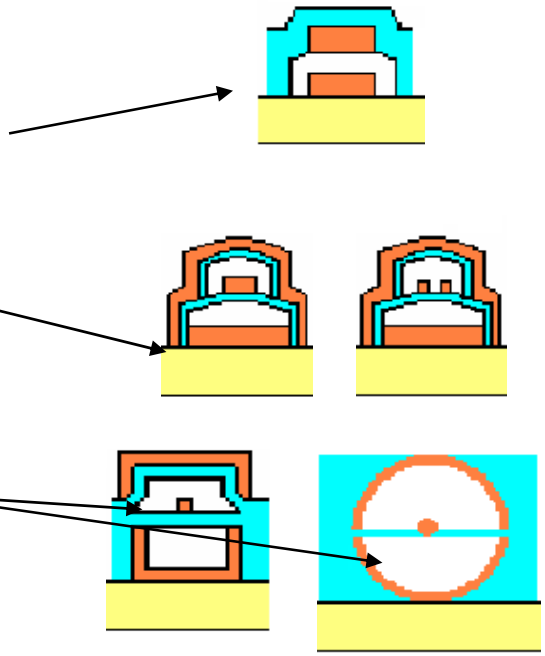
- Test chips with 4x10Gb/s transmitters and cross-talk cancellation to test air cavity line performance

Future Multilayer Channel Buildup

* Low loss signal line build-up on multilayer boards uses existing infrastructure
* Channel cross-sectional area determines loss and channel density
  - » Unshielded, nonplanar structures easy to build, higher loss
  - » Shielded structures have lower loss, but larger cross-sectional area
  - » Buildup process gives nonplanar lines
  - » Inlay processes are more valuable, more difficult to make

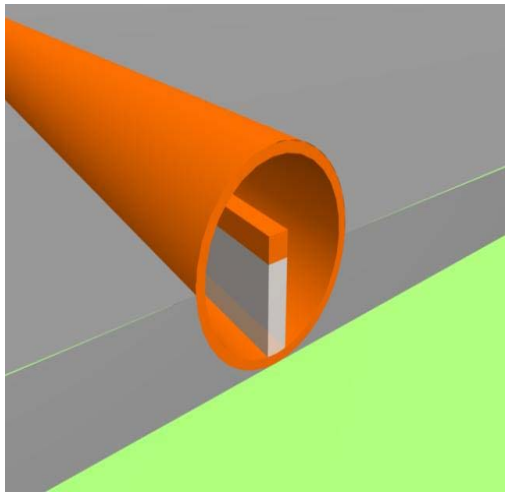


Multilayer board vias
From www.ibiden.co.jp

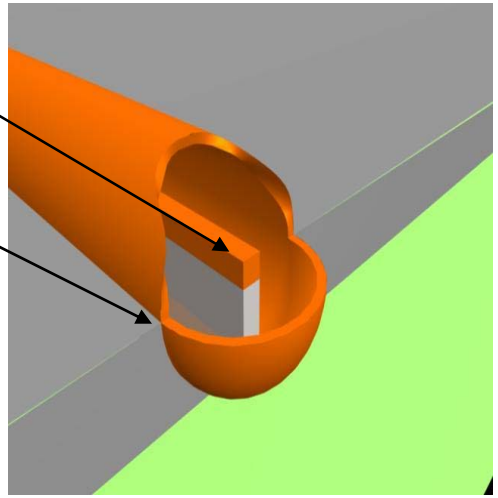


Future Imprint Lithography: Complex geometries

- **Coaxial geometry minimizes crosstalk noise and radiation losses**
- **Channel geometries with complex shapes can be built using imprint lithography**
- **Routing terminations and chip connections can be more easily defined using imprint**
- **Smooth, rounded transitions will minimize reflections and maximize power transmission**



Proposed Coaxial Line



Proposed Vertical/Horizontal Connection

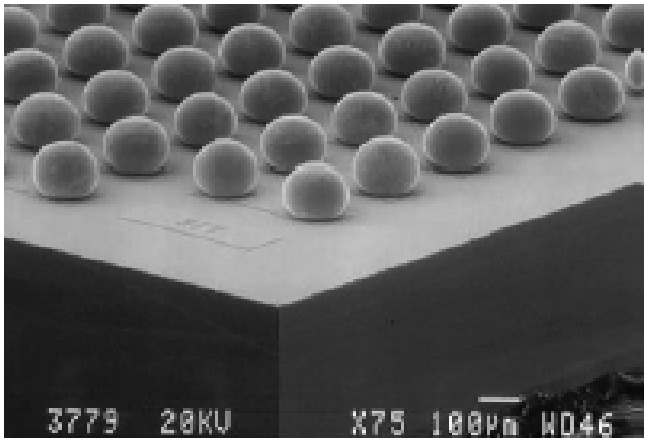
High Performance Chip-to-Substrate Connections

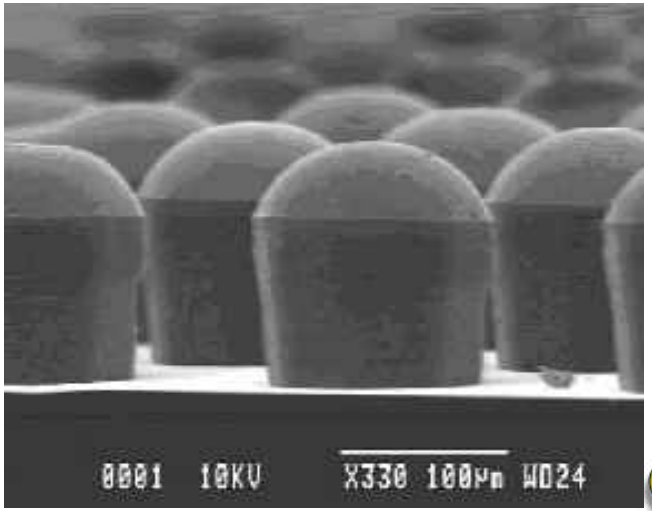
Tyler Osborn

Introduction

* Flip-Chip Interconnects are a critical interface between the IC and system
* Large numbers are connections are made over a small surface area
  - » 1,000 – 10,000 I/O
  - » Typical Die is ~ 225 mm^2
* Solder melt-cast connections are the industry standard

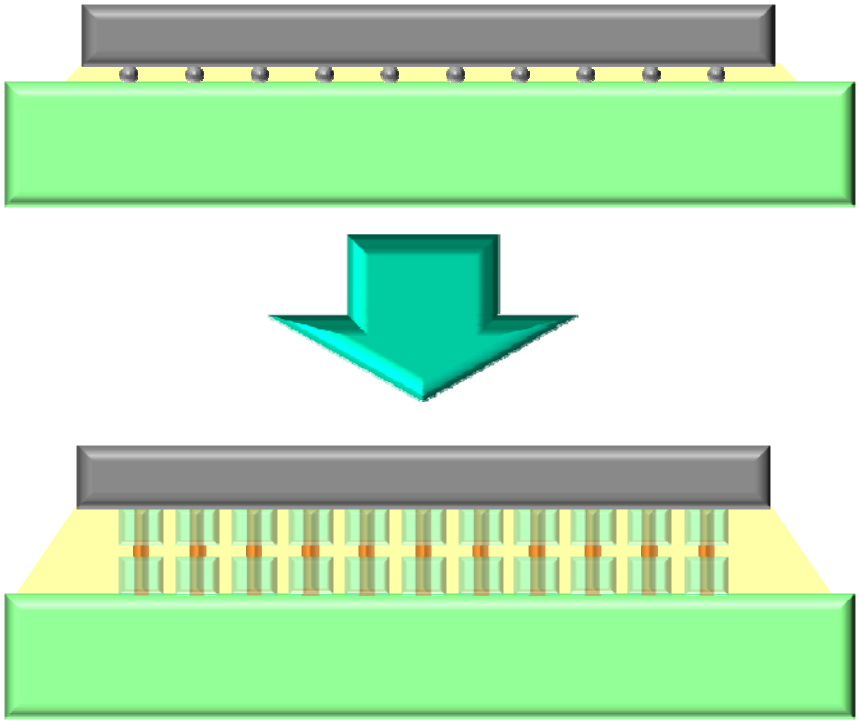
Year	2010	2015	2020
Area Array Pitch (µm)	120	100	85
I/O per cm^2	7000	10000	14000
Off Chip Freq. (GHz)	9.5	29.1	72.4





All-Copper Approach

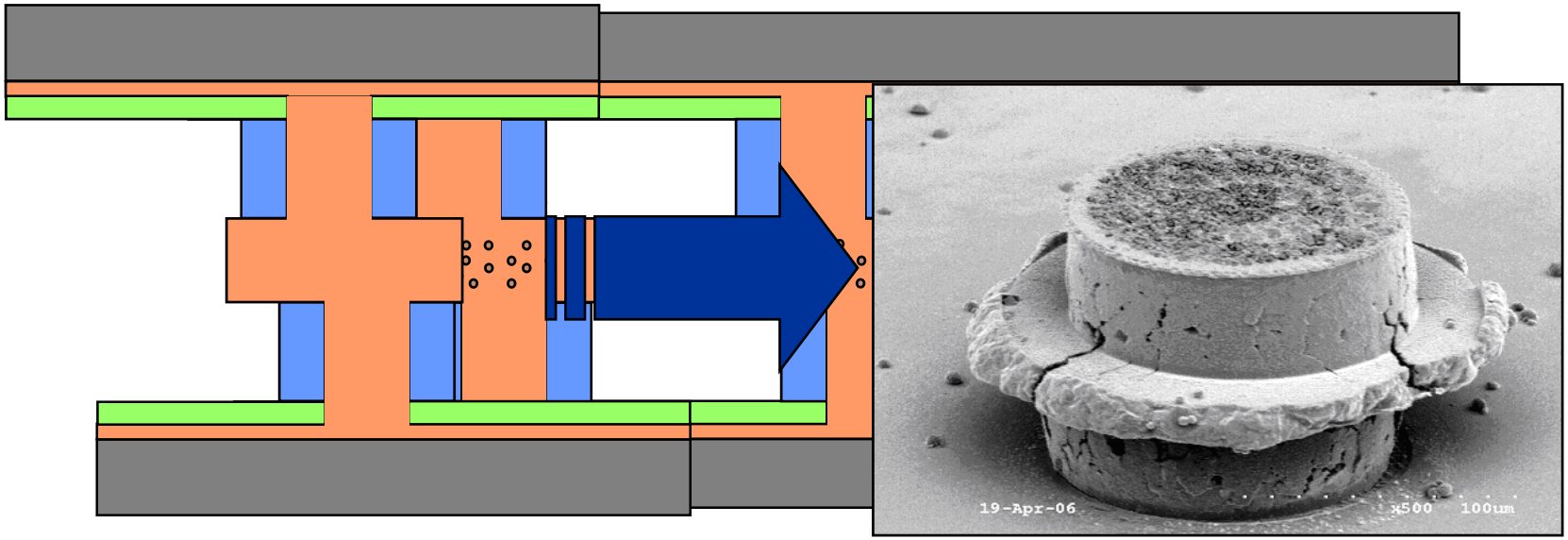
* Replace solder with copper:
  - » Electrical improvement
  - » Thermo-Mechanical
* Copper-to-copper bonding:
  - » Low Cost
  - » Low Temperature
  - » Mechanical Compliance
* Current SnPb and SnAgCu:
  - » Undesirable properties:
    - Limited (H:W) aspect ratio
    - Brittle intermetallics
    - High capacitance (underfill)
    - Low electromigration resistance
  - » Desirable properties:
    - Low processing temperature
    - Tolerance- x-y misalignment
    - Tolerance to height variation



Addition of underfill to Cu pillar system is possible for reliability

All Copper Interconnects

1. Flip Chip Alignment
2. Electroless Plating
3. Low T Annealing
4. Shear Testing



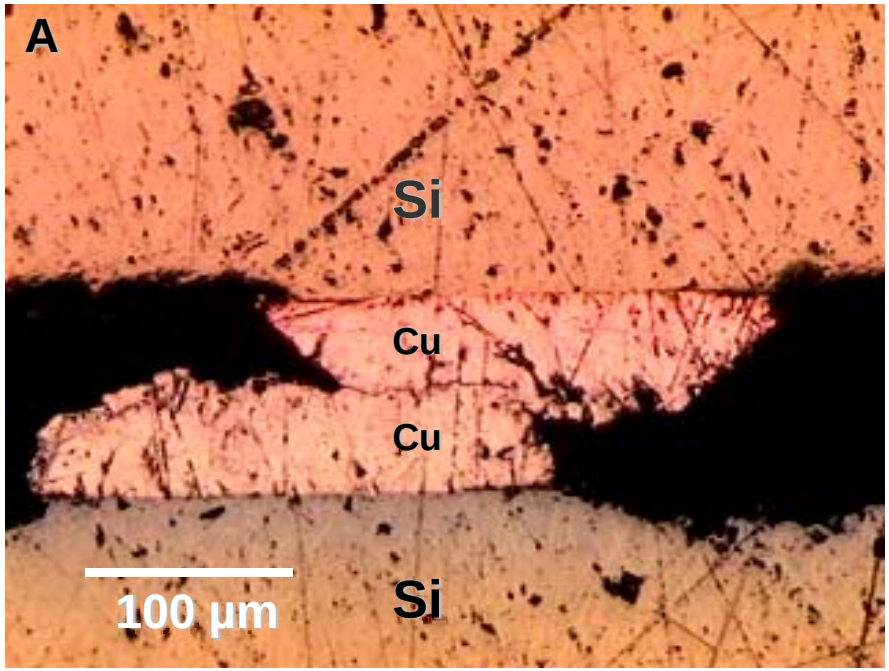
SiO_2 Avatrel
Cu Si

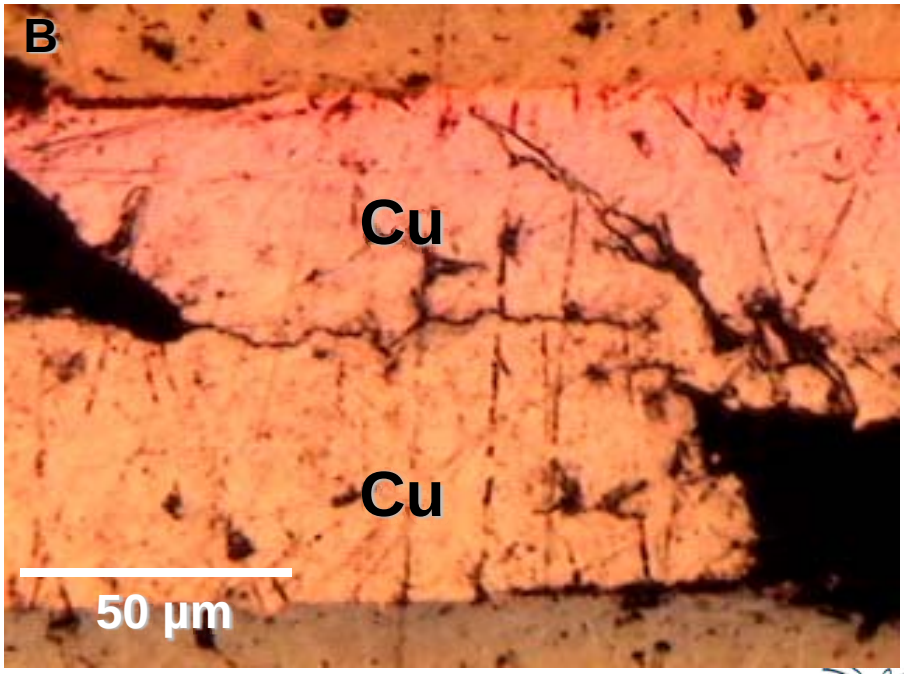
Patent Pending Process:

Integrated Circuit Interconnection Devices and Methods
Ate He, Tyler Osborn, Paul Kohl. September 2006
US Patent Application # 20080073795

Bonding Mechanism

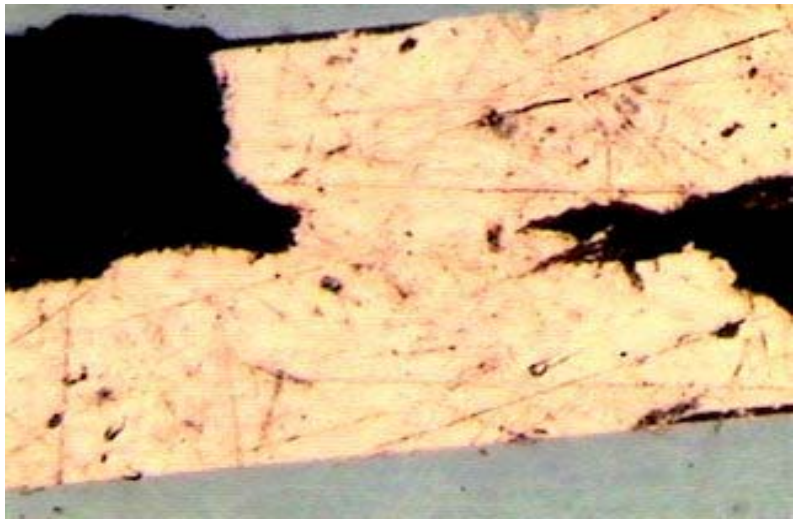
* No anneal: Unbonded interface between electrolessly plated pillars prior to annealing processes

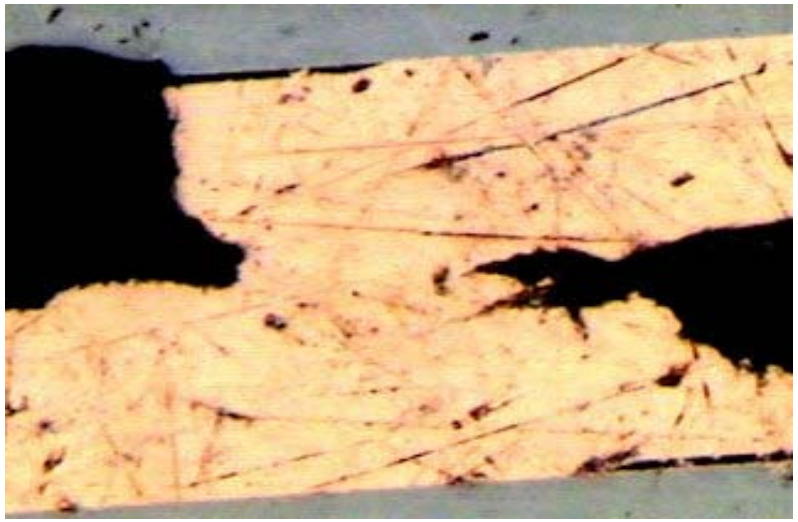




Bonding Mechanism

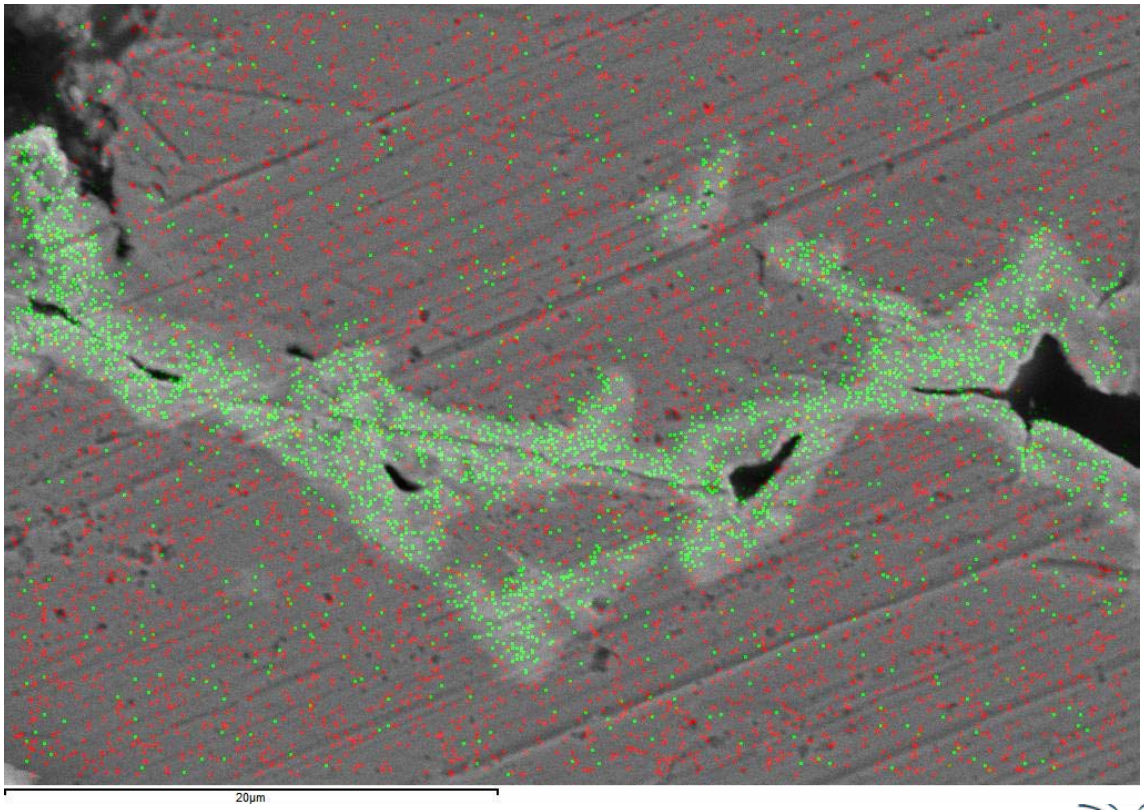
» Additional annealing at 180C for 30 minutes, interface is eliminated



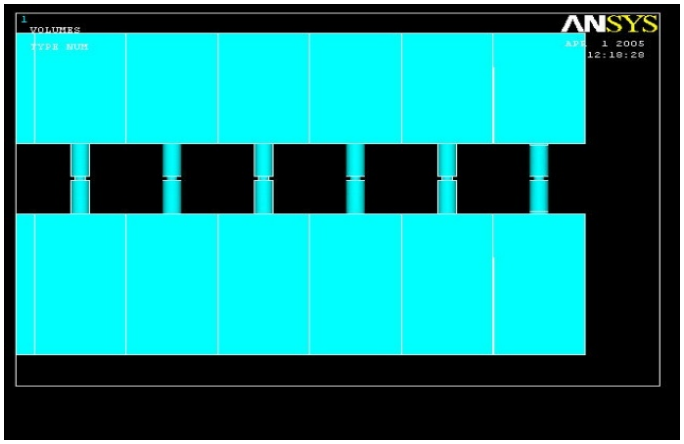


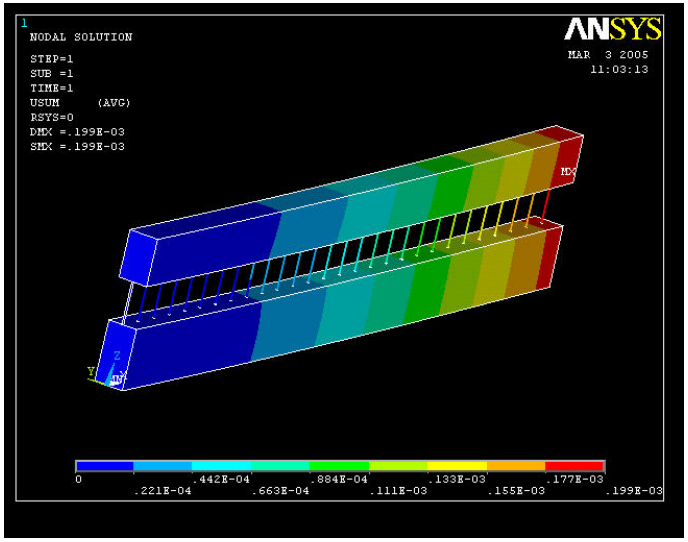
Will Other Metals Bond?

* Electroless gold
* Annealed to form joint
* Gold-Gold seam closed



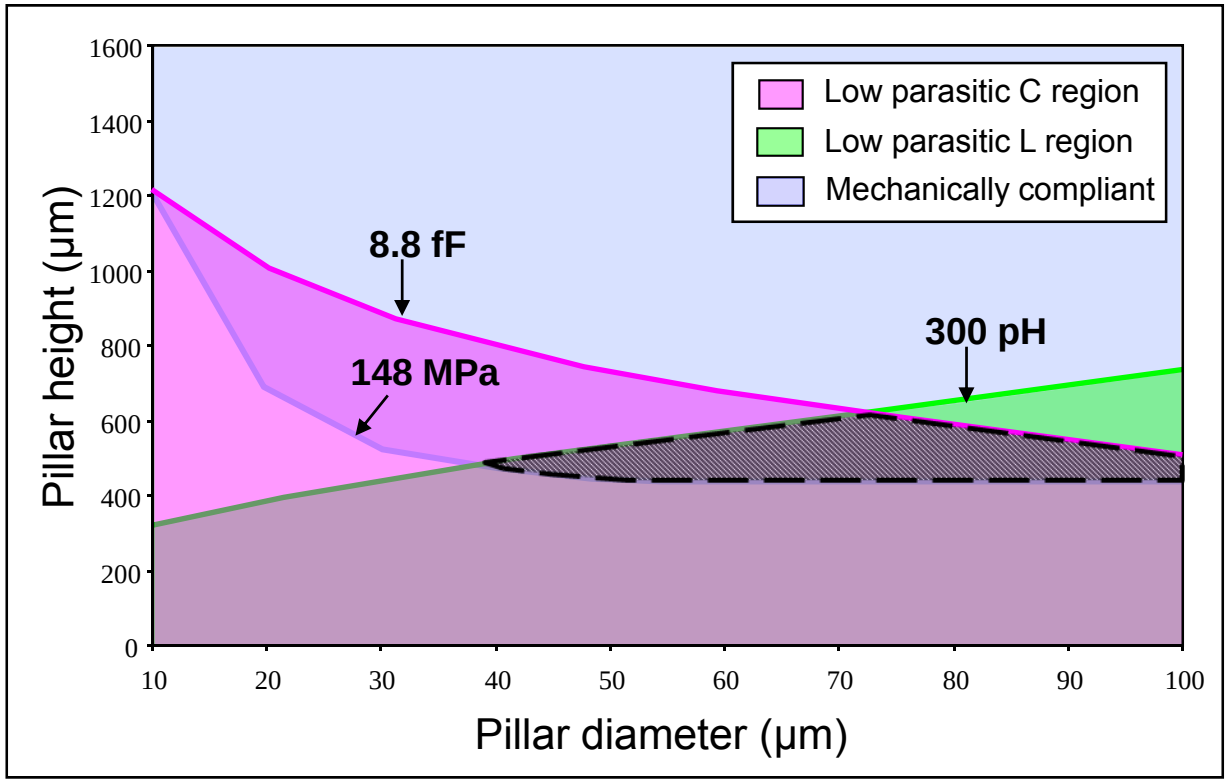
Model Results

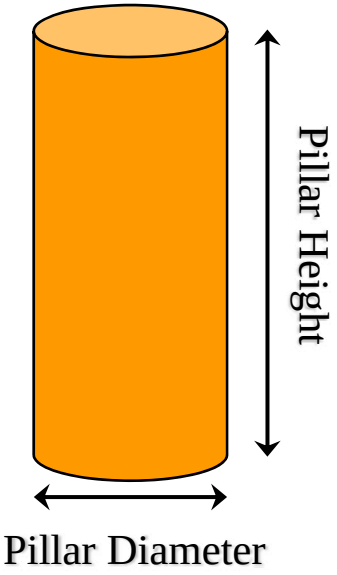




* The stress state within the copper pillar and at the chip & substrate surface is a function of:
  - » Position
  - » Shape
  - » ‘Collar’ Material

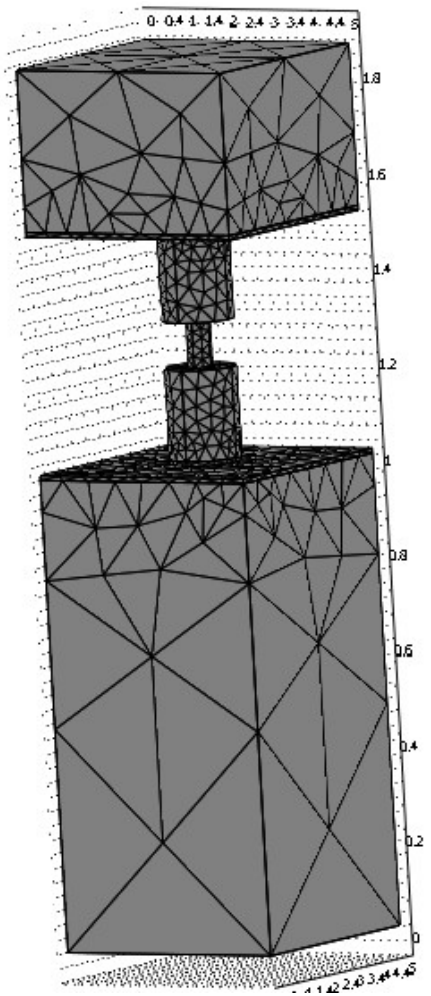
GPD Model Results



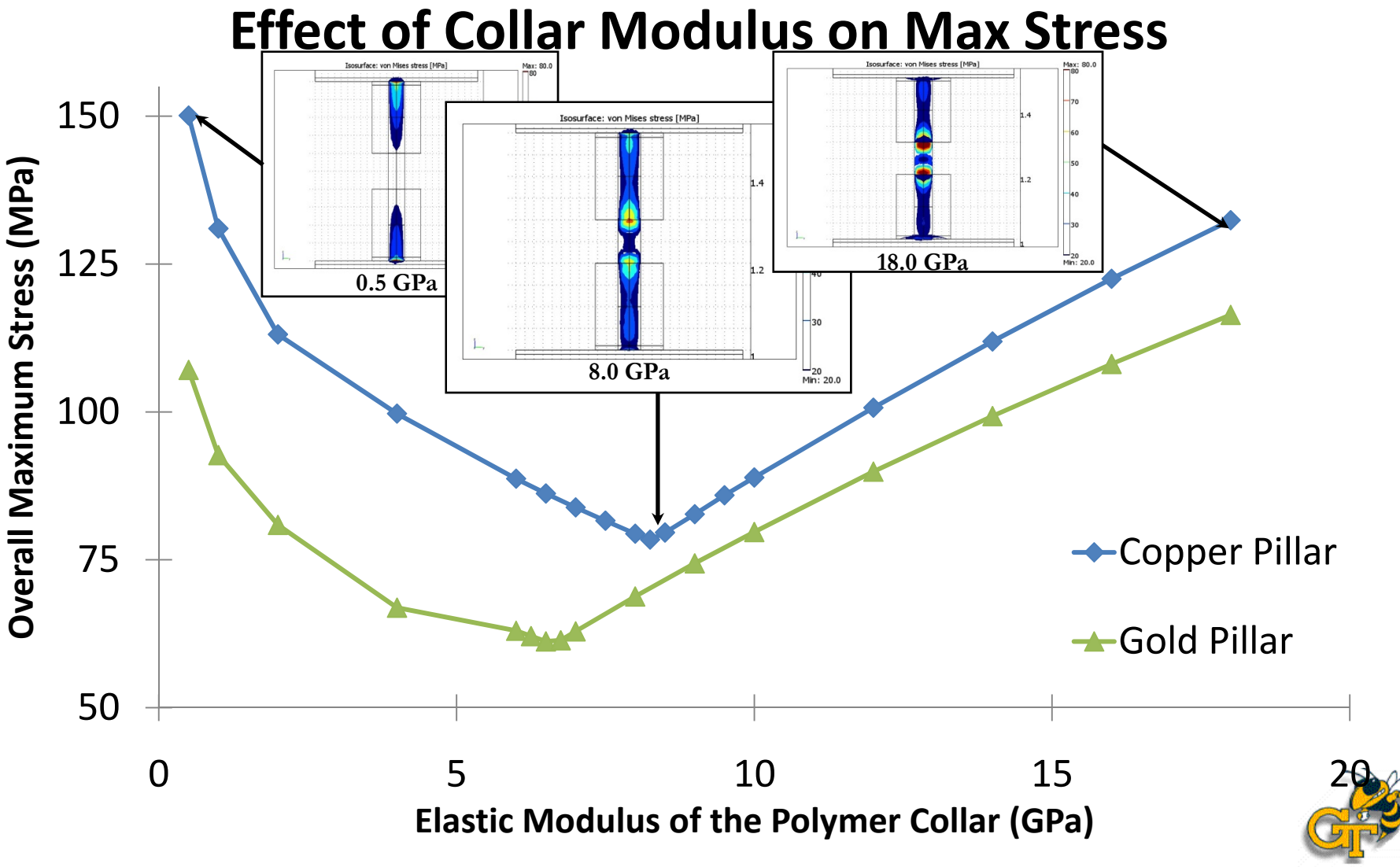


Single Pillar Model

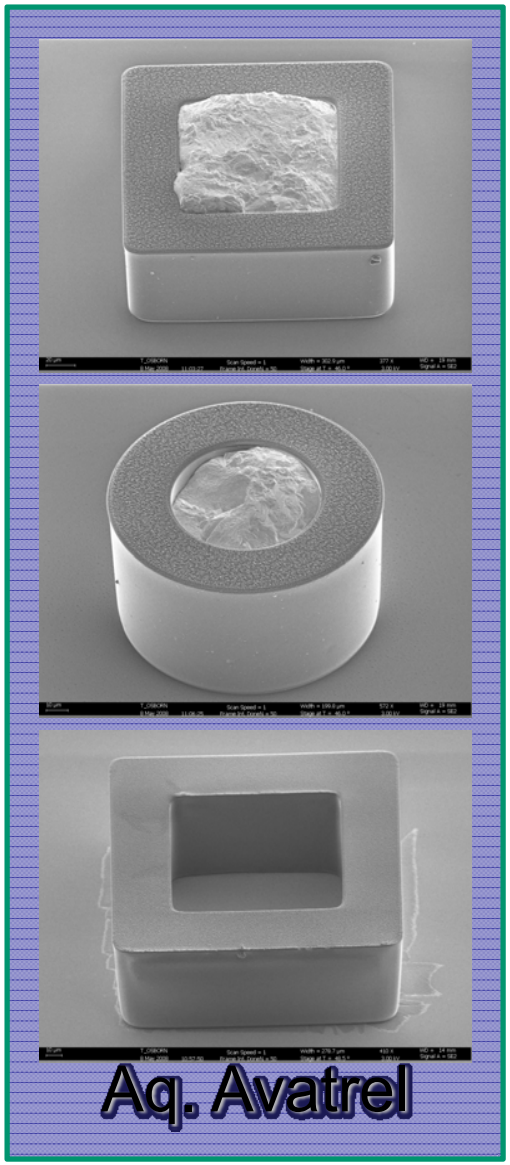
- A single pillar model - mimics previous GPD model
- Correctly matches maximum stresses for all GPD results
- **TARGET:** Lower stress from 148 MPa (adhesive failure) to below ‘solder & low-k’ values.
- **NEW GOAL:** Yield stress of solder is the only agreed upon value.
  - SnAgCu ~ 50 MPa
  - Eutectic SnPb ~ 25 MPa

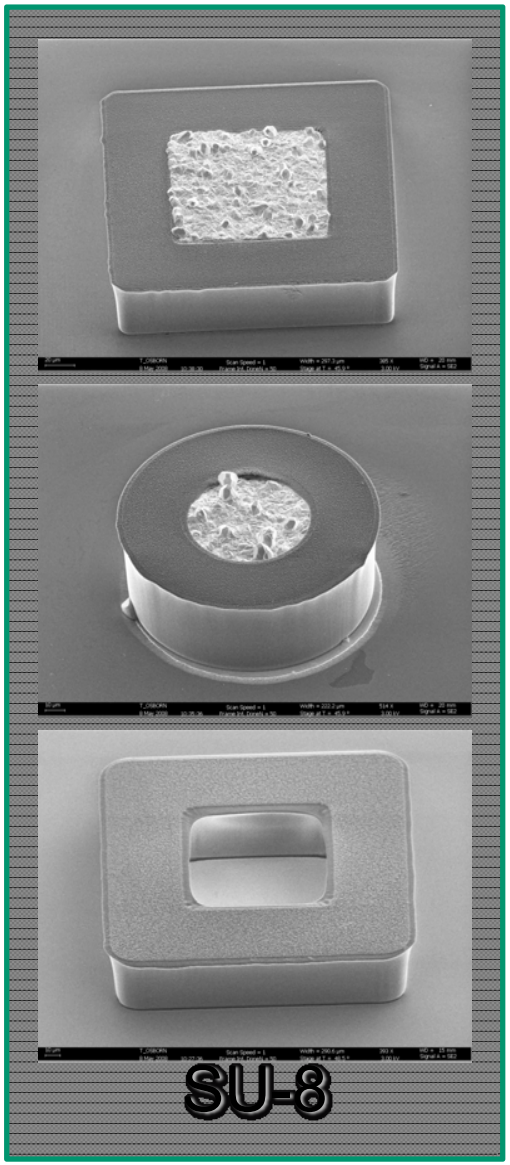


Results – Single Polymer Collar

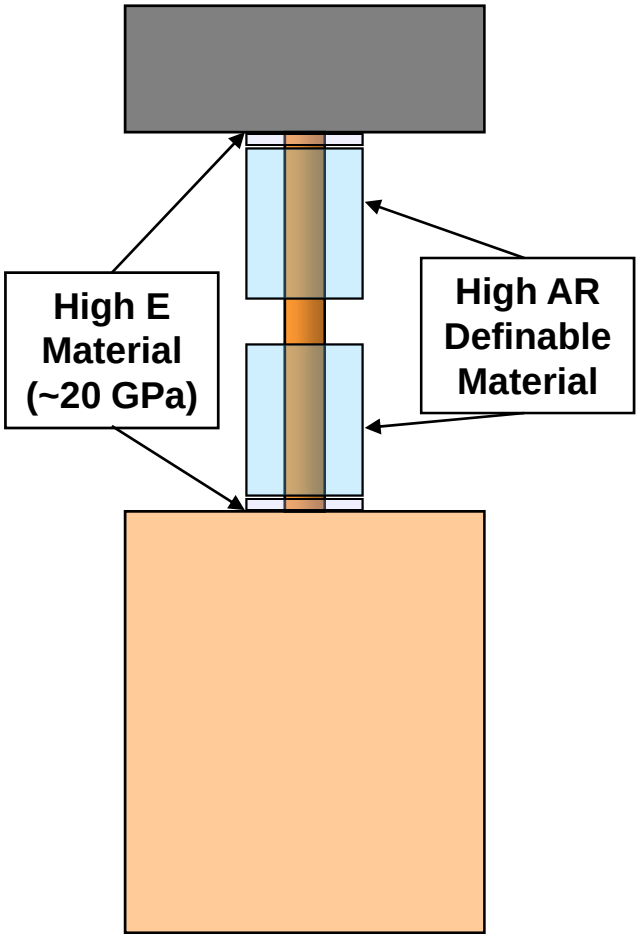


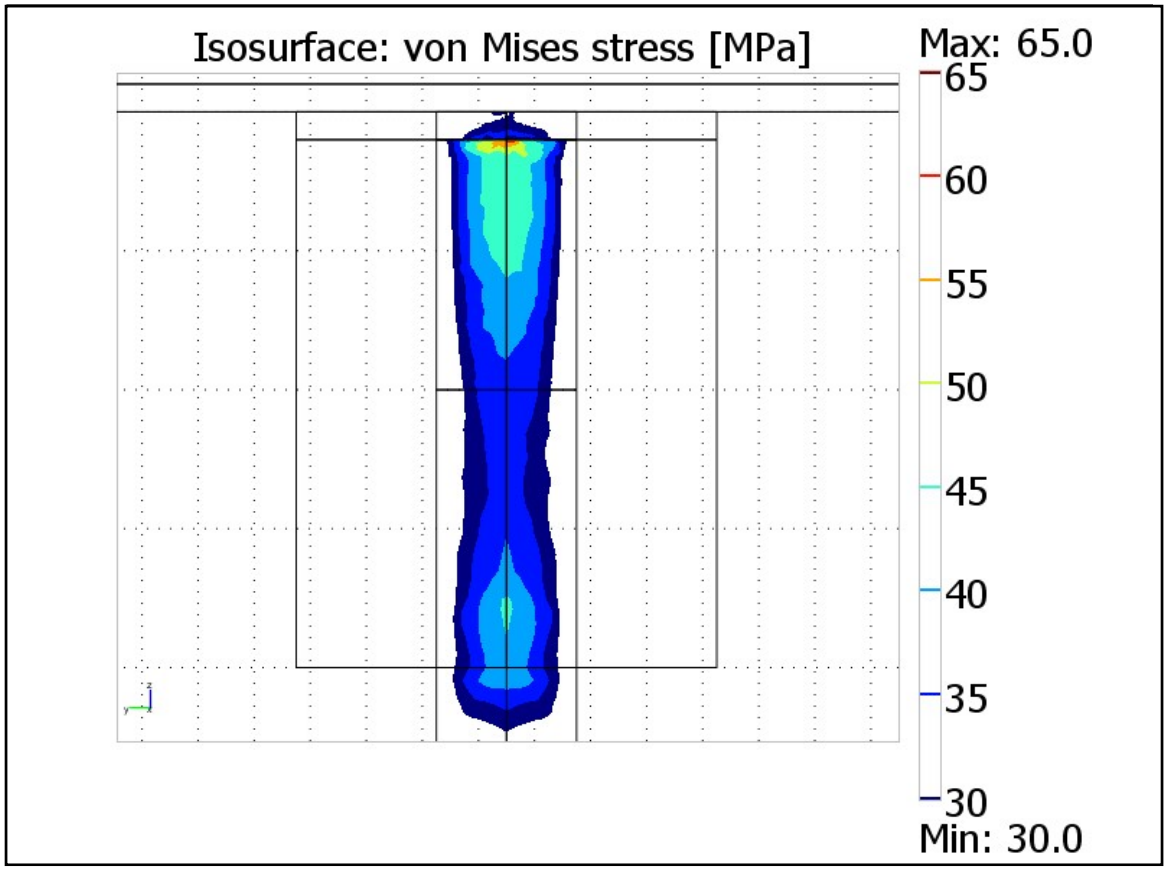
Comparing Polymer Collars





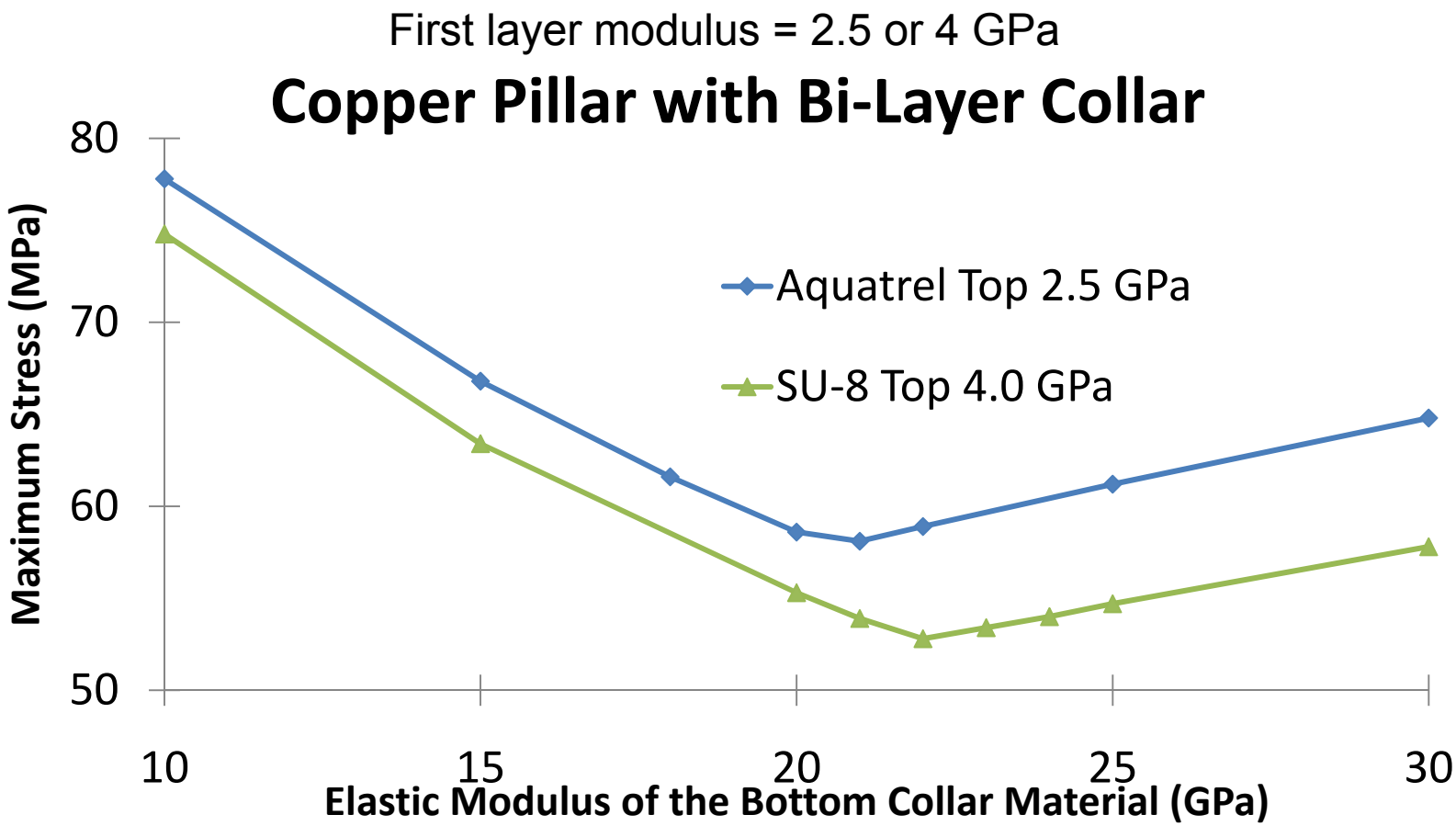
Bi-Layer Collar Results





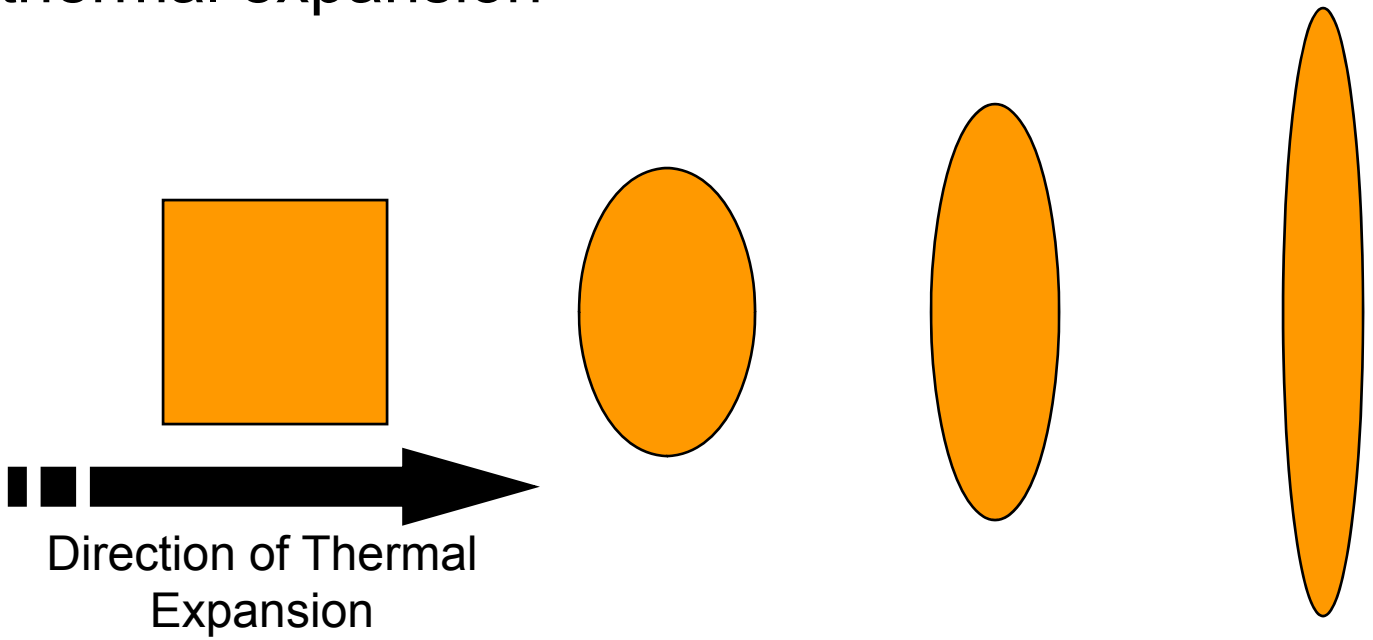
SU-8 Top Collar with E=50 GPa Base

Bi-Layer Collar Results

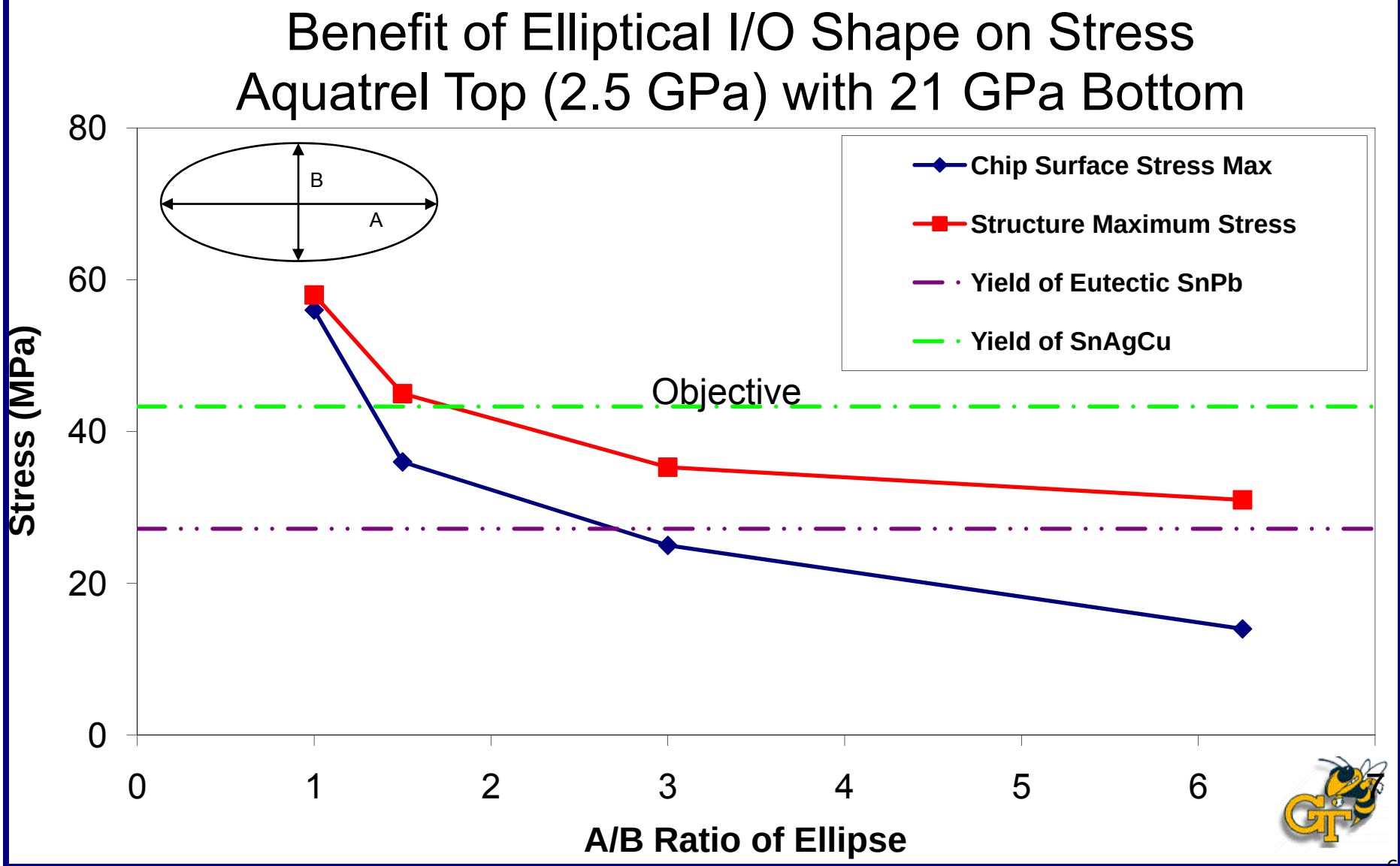


Changing Shape

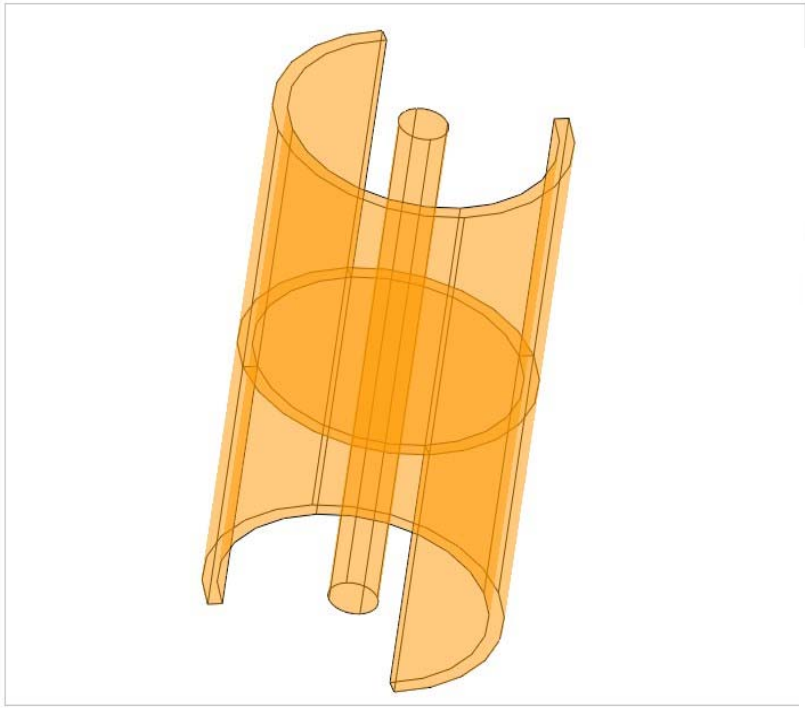
- Cylindrical I/O has high stress point at leading and tailing edge of pillar.
- Distribute the stress at the chip interface over a greater area by using *Ellipse or Square I/O*
- **KEY:** Align the broad face directly in the direction of thermal expansion

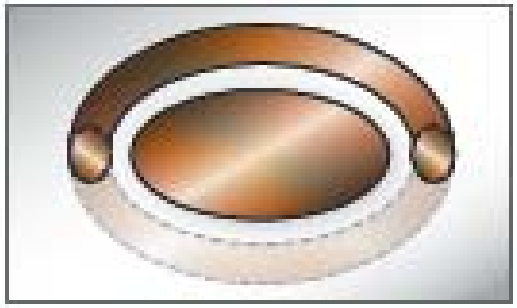


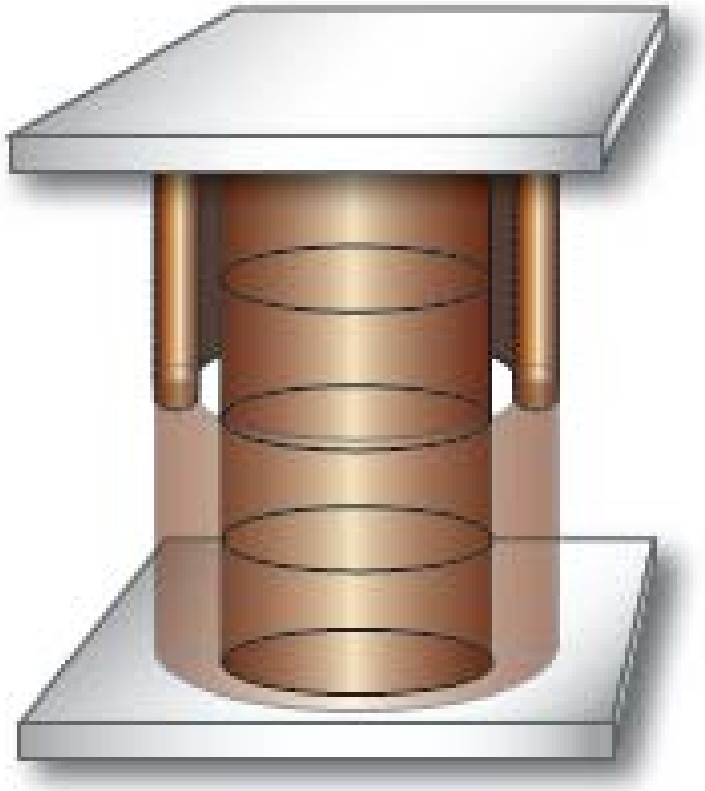
Ellipse Effect Results



High Frequency, Shielded I/O

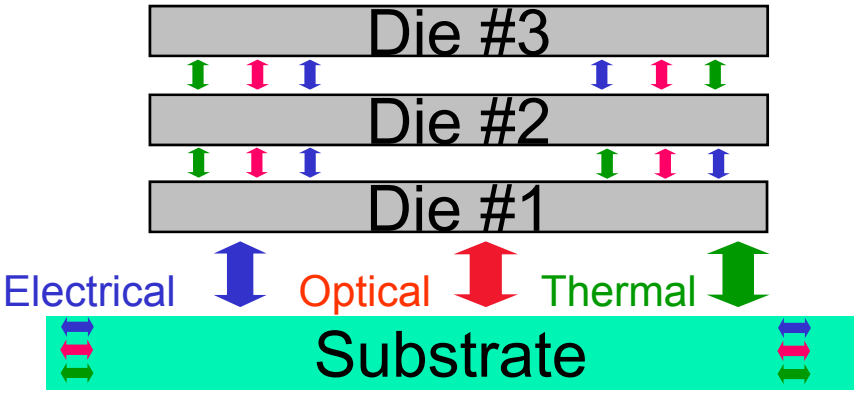


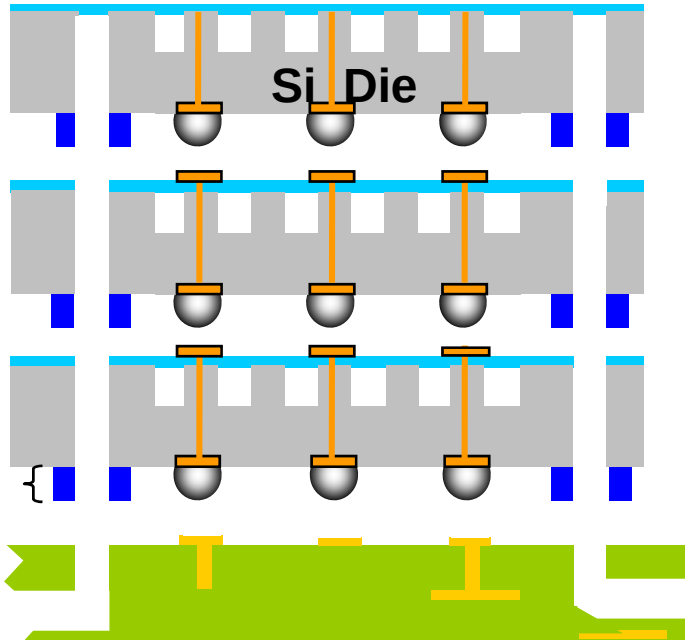




Future Insulation, Cooling, and Conductors

3-D Electronics: Short Wires





Comments

* Transistor scaling is slowing
* Need for Bandwidth (not clock speed) is increasing due to applications
* Critical needs:
  - » Very low Permittivity and Loss materials
  - » Ballistic transport in conductors (no scattering)
  - » Advanced cooling (Fluids-to-the-chip)
  - » Simple, high-yield processes